One step a-Si:H TFT’S with PECVD SiO$_x$N$_y$ gate insulator

K.F. Albertin and I. Pereyra

LME, EPUSP, University of São Paulo,
CEP 5424-970, CP61548, São Paulo, SP, Brazil.

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Amorphous silicon thin film transistors (TFT’s), utilizing silicon dioxide (SiO$_2$), silicon oxynitride (SiO$_x$N$_y$) and silicon nitride (Si$_3$N$_4$) obtained by PECVD as gate insulating material, are fabricated through just one masking process and characterized by drain current vs drain voltage and by drain current vs gate voltage ($I_{ds}$ vs. $V_{ds}$, and $I_{ds}$ vs. $V_{gs}$) measurements.

Keywords: One mask step; silicon oxynitride; thin film transistors.

Son fabricados con apenas una etapa de fotolitografía transistores de capa fina de silicio amorfo utilizando, como material dieléctrico de compuerta, dióxido de silicio (SiO$_2$), oxinitruro de silicio (SiO$_x$N$_y$) y nitruro de silicio (Si$_3$N$_4$) creados por PECVD. Los dispositivos son caracterizados por medio de mediciones de corriente de dreno vs voltaje de dreno y corriente de dreno vs voltaje de compuerta ($I_{ds}$ vs. $V_{ds}$, y $I_{ds}$ vs. $V_{gs}$)

Descriptores: fotolitográfica; oxinitruro de silicio; transistores de capa fina

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1. Introduction

Thin Film Transistors (TFT) with amorphous silicon nitride gate dielectric (SiN$_x$) and amorphous silicon (a-Si:H) active layer are emerging as the most utilized switching device for active matrix liquid crystal displays (AMLCD’s) [1–5]. However, low channel field effect mobility and charge trapping in the a-Si:H/SiN$_x$ interface are described as the major challenges for the improvement of the TFT electrical characteristics [6]. So studies are oriented to alternative dielectrics, among them silicon dioxide (SiO$_2$), which in spite of its good insulating properties can not be utilized as a single layer due to its high interface state density with a-Si:H. Some authors utilize an N$_2$ or an NH$_3$ plasma treatment of the SiO$_2$ layer to incorporate nitrogen at the a-Si:H/SiO$_2$ interface [7]. Also some works have reported the use of SiO$_x$N$_y$ in TFT’s as double insulating gate (SiN$_x$/SiO$_x$N$_y$) [8]. In previous [9] works we studied the characteristics of MOS capacitors utilizing SiO$_x$N$_y$ dielectric layer, with nitrogen concentration varying from SiO$_2$ to Si$_3$N$_4$, and we identified the composition, which leads to the best interface properties. In this work we fabricate and characterize amorphous TFT’s with three different dielectric layers (SiO$_2$, SiO$_x$N$_y$, and Si$_3$N$_4$), intending to identify the dielectric film that presents the best insulating/a-Si:H interface properties.

2. Experiment

The bottom gate, just one masking step TFT’s fabrication process is schematized in Fig. 1.

The devices were fabricated on corning glass, utilizing a chromium electrode as gate contact (300 nm), SiO$_2$N$_y$ (90 nm), SiO$_2$ (70 nm) and Si$_3$N$_4$ (70 nm, ~ 31 N at %) as insulating layer, undoped a-Si:H active layer (100nm) and aluminum drain and source contacts (300 nm). Both the insulating layer and the active layer were deposited by the PECVD technique; the deposition conditions for all the utilized films are shown in Table I.

<table>
<thead>
<tr>
<th>Film</th>
<th>SiH$_4$ (sccm)</th>
<th>N2O (sccm)</th>
<th>N2 (sccm)</th>
<th>Pressure (mTorr)</th>
<th>Temperature (°C)</th>
<th>Power (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>3</td>
<td>39</td>
<td>—</td>
<td>17</td>
<td>320</td>
<td>100</td>
</tr>
<tr>
<td>SiO$_x$N$_y$</td>
<td>3</td>
<td>3</td>
<td>36</td>
<td>17</td>
<td>320</td>
<td>100</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>3</td>
<td>—</td>
<td>39</td>
<td>17</td>
<td>320</td>
<td>100</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>10</td>
<td>—</td>
<td>400</td>
<td>250</td>
<td>100</td>
<td>50</td>
</tr>
</tbody>
</table>

In Fig. 2 the typical output characteristics for transistors with a channel width W of 2 mm and a channel length L of 20 µm, with SiO$_2$, SiO$_x$N$_y$ and Si$_3$N$_4$, gate dielectric layer, respectively are shown.

It is observed that the drain current values vary with the gate voltage applied, and a well-defined saturation region is observed for all the devices and geometries. In this way the transconductance is well defined. It is observed that the TFT with SiO$_x$N$_y$ gate dielectric presents the highest drain current. It is also observed that the drain current is different from zero for zero drain voltage, indicating that these devices present a leakage current ($I_g$), probably due to pinholes in the dielectric layer.

In Fig. 3 the gate current vs gate voltage ($I_{gs}$ vs $V_{gs}$) characteristic for the three insulating layers are shown; the highest
The series resistance is associated with the amorphous silicon film thickness and with the contact resistance, and it af-
The threshold voltage ($V_{th}$) values were obtained by the extrapolation of the square root of the drain saturation current as a function of the gate voltage; the values obtained were 4.6 V, 3.8 V and 2.2 V for SiO$_2$, SiO$_2$N$_y$, and Si$_3$N$_4$ and gate insulator TFT’s respectively. These values are compatible with those reported in the literature for standard bottom gate TFT (between 2-4 V) [10]. Finally we extracted the channel mobility in saturation ($\mu$) regime, using the saturation drain current expression $I_{ds(sat)} = \beta [(V_g - V_{th})^2 - V_{ds}^2/2]$, where $\beta = (W/L)C_{ox}\mu$, and Cox is the dielectric capacitance. We found a channel mobility of 0.05, 0.3 and 0.03 cm$^2$/V s for TFT’s using SiO$_2$, SiO$_2$N$_y$, and Si$_3$N$_4$ respectively. The highest value was obtained for the SiOxNy gate dielectric TFT, which probably is correlated with better insulator/a-Si:H interface properties, which at a time can be related with the lower mechanical stress associated with this film, as observed in previous works [12].

4. Conclusions

Bottom gate amorphous silicon hydrogenated based TFT’s, with silicon dioxide SiO$_2$, SiO$_2$N$_y$ and Si$_3$N$_4$ insulating layer and undoped amorphous silicon active layer were fabricated through a one deposition and one masking step process. A well-defined transistor action was obtained for all devices. We found the highest mobility for the silicon oxynitrde gate insulator TFT, a result which can be related to the lower mechanical stress associated with this film leading to better insulator/a-Si:H interface properties.

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