One step a-Si:H TFT'S with PECVD SiO_xN_y gate insulator

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Amorphous silicon thin film transistors (TFT's), utilizing silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) and silicon nitride (Si_3N_4) obtained by PECVD as gate insulating material, are fabricated through just one masking process and characterized by drain current vs drain voltage and by drain current vs gate voltage (I_{ds} vs. V_{ds} and I_{ds} vs. V_{gs}) measurements.

Keywords: One mask step; silicon oxynitride; thin film transistors.

Son fabricados con apenas una etapa de fotolitografía transistores de capa fina de silicio amorfo utilizando, como material dieléctrico de compuerta, dióxido de silicio (SiO_2), oxinitruro de silicio (SiO_xN_y) y nitruro de silicio (Si_3N_4) crecidos por PECVD. Los dispositivos son caracterizados por medio de mediciones de corriente de dreno vs voltaje de dreno y corriente de dreno vs voltaje de compuerta (I_{ds} vs. V_{ds} y I_{ds} vs. V_{gs})

Descriptores: fotolitográfica; oxinitruro de silicio; transistores de capa fina

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1. Introduction

Thin Film Transistors (TFT) with amorphous silicon nitride gate dielectric (SiN_x) and amorphous silicon (a-Si:H) active layer are emerging as the most utilized switching device for active matrix liquid crystal displays (AMLCD's) [1–5]. However, low channel field effect mobility and charge trapping in the a-Si:H/SiN_x interface are described as the major challenges for the improvement of the TFT electrical characteristics [6]. So studies are oriented to alternative dielectrics, among them silicon dioxide (SiO_2), which in spite of its good insulating properties can not be utilized as a single layer due to its high interface state density with a-Si:H. Some authors utilize an N_2 or an NH_3 plasma treatment of the SiO_2 layer to incorporate nitrogen at the a-Si:H/SiO_2 interface [7]. Also some works have reported the use of SiO_xN_y in TFT's as double insulating gate (SiN_x/SiO_xN_y) [8]. In previous [9] works we studied the characteristics of MOS capacitors utilizing SiO_xN_y dielectric layer, with nitrogen concentration varying from SiO_2 to Si_3N_4, and we identified the composition, which leads to the best interface properties. In this work we fabricate and characterize amorphous TFT's with three different dielectric layers (SiO_2, SiO_xN_y and Si_3N_4), intending to identify the dielectric film that presents the best insulating/a-Si:H interface properties.

2. Experiment

The bottom gate, just one masking step TFT's fabrication process is schematized in Fig. 1.

The devices were fabricated on corning glass, utilizing a chromium electrode as gate contact (300 nm), SiO_xN_y (90 nm), SiO_2 (70 nm) and Si_3N_4 (70 nm, $\sim$ 31 N at %) as insulating layer, undoped a-Si:H active layer (100nm) and aluminum drain and source contacts (300 nm). Both the insulating layer and the active layer were deposited by the PECVD technique; the deposition conditions for all the utilized films are shown in Table I.

TABLE I. Deposition conditions for dielectric layers and the active layer of the TFT's.

Film	SiH4 (sccm)	N2O (sccm)	N2 (sccm)	Pressure (mTorr)	Temperature (°C)	Power (Watts)
SiO_2	3	39	—	17	320	100
SiO_xN_y	3	3	36	17	320	100
Si_3N_4	3	—	39	17	320	100
a-Si:H	10	—	—	400	250	10

The thickness of the a-Si:H and SiO_xN_y films was measured in an Alpha Step 500 Tencor surface profiler. The drain current vs drain voltage (I_{ds} vs V_{ds}) and the drain current vs gate voltage (I_{ds} vs V_{gs}) characteristic curves for these devices were obtained in an HP 4145B Parameter Analyzer.

3. Results

In Fig. 2 the typical output characteristics for transistors with a channel width W of 2 mm and a channel length L of 20 μm, with SiO_2, SiO_xN_y and Si_3N_4, gate dielectric layer, respectively are shown.

It is observed that the drain current values vary with the gate voltage applied, and a well-defined saturation region is observed for all the devices and geometries. In this way the transconductance is well defined. It is observed that the TFT with SiO_xN_y gate dielectric presents the highest drain current. It is also observed that the drain current is different from zero for zero drain voltage, indicating that these devices present a leakage current (I_g), probably due to pinholes in the dielectric layer.

In Fig. 3 the gate current vs gate voltage ($I_{gx}V_{gs}$) characteristics for the three insulating layers are shown; the highest

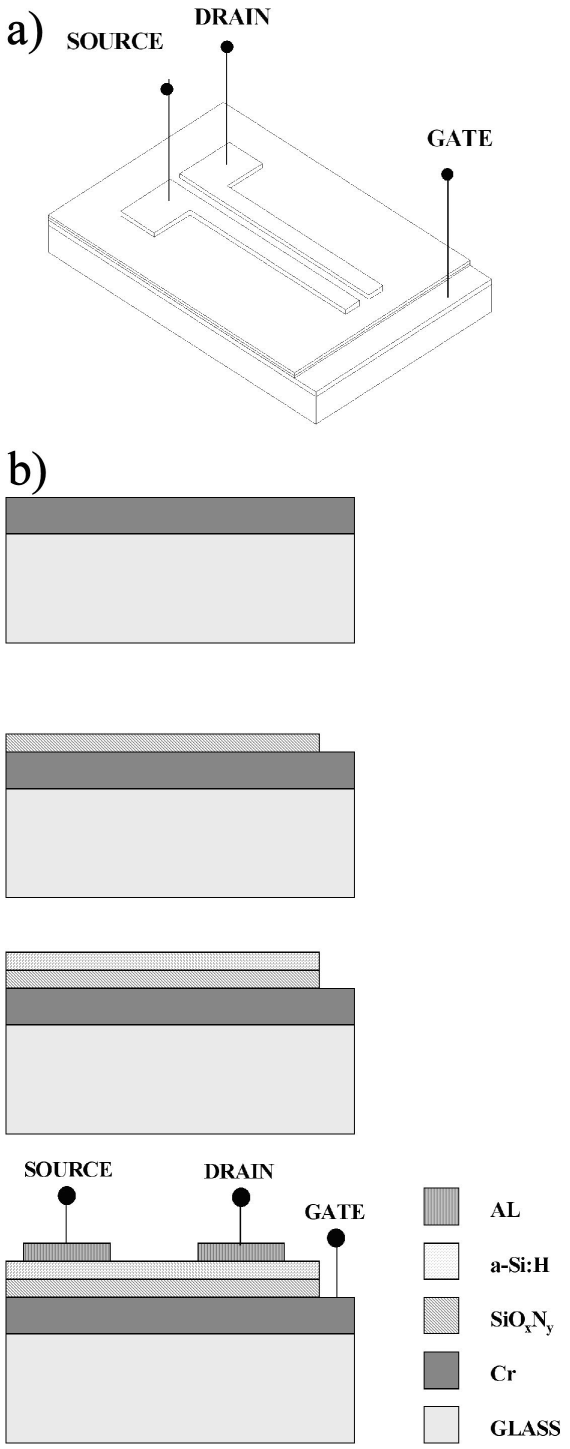

FIGURE 1. Thin film transistor (a) bottom gate structure and (b) fabrication steps.

I_G value obtained was for the TFT with SiO_xN_y gate dielectric. Thus for an appropriate parameter extraction, the I_{ds} values should be corrected for leakage current. Also the parasitic drain and source series resistance may have a considerable effect on the current - voltage transistor characteristics for a-Si:H TFT's [10].

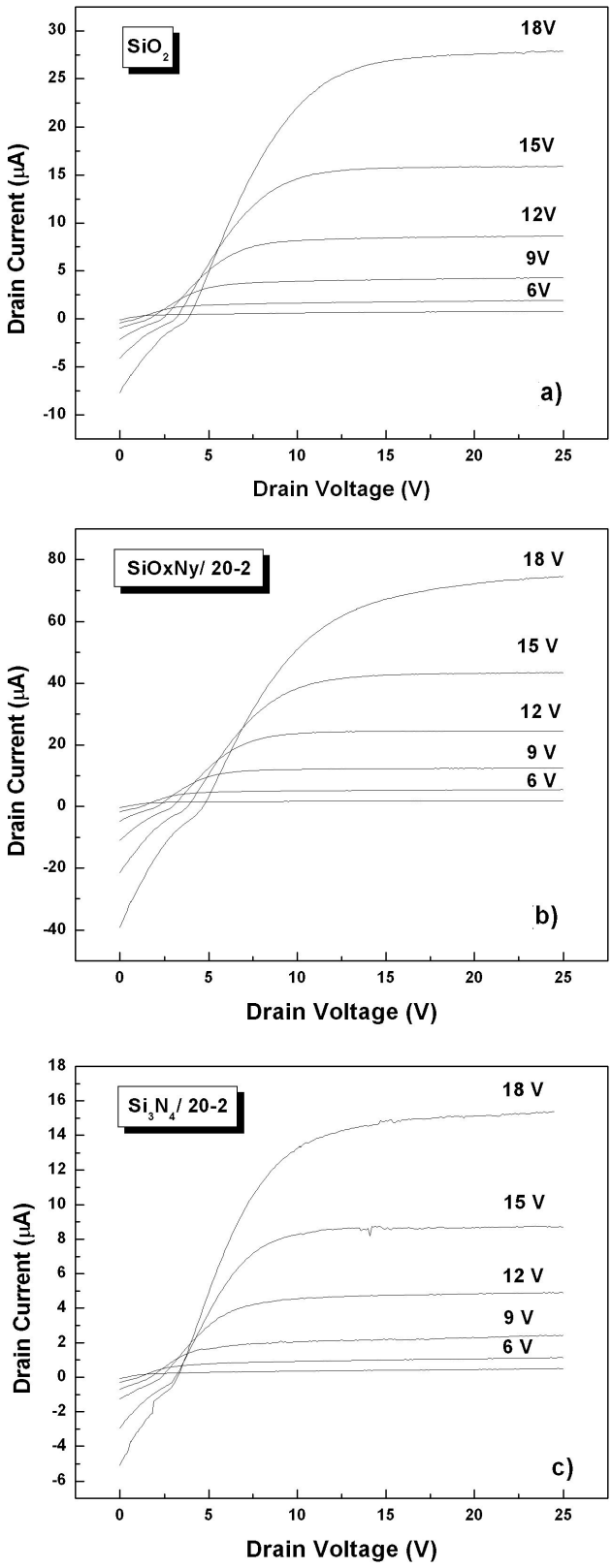

FIGURE 2. Thin Film Transistor characteristic curve (I_{ds} vs. V_{gs}) for $W = 2$ mm and $L = 20$ μm a) SiO_2, b) SiO_xN_y, c) Si_3N_4.

The series resistance is associated with the amorphous silicon film thickness and with the contact resistance, and it af-

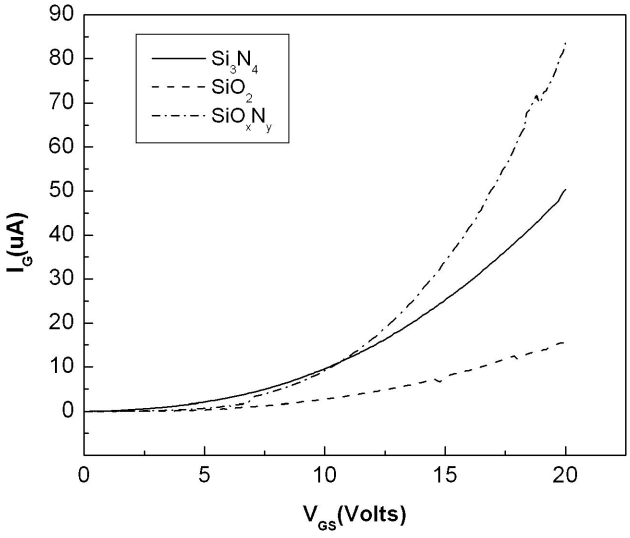

FIGURE 3. Gate current vs gate voltage for SiO_2, SiO_xN_y, and Si_3N_4 insulator layer TFT's.

fects the extraction of the channel mobility and increases the threshold voltage value [11]. The amorphous silicon thickness contribution to R_s was estimated from the amorphous silicon resistivity ($\sim 6.2 \times 10^4$ Ω cm), leading to a value of 2.3×10^3 Ω, which means that for the highest I_{ds} value obtained it will give a voltage loss of 0.1V, thus having a negligible effect on the I_{ds} vs. V_{ds} characteristics. Regarding to the contact resistance contribution, the non-linear behavior of I_{ds} for small V_{ds} suggests that the Al/a-Si:H contacts are in fact rectifying Schottky barriers; n+ source and drain regions would be necessary in order to guarantee good ohmic contacts. In this way, the V_{ds} loss in these contacts is difficult to compute, thus preventing series resistance correction. Consequently, the extracted mobility values are underestimated and the threshold voltage ones are overestimated.

The threshold voltage (V_{th}) values were obtained by the extrapolation of the square root of the drain saturation current as a function of the gate voltage; the values obtained were 4.6 V, 3.8 V and 2.2 V for, SiO_2, SiO_xN_y and Si_3N_4 and gate insulator TFT's respectively. These values are compatible with those reported in the literature for standard bottom gate TFT (between 2-4 V) [10]. Finally we extracted the channel mobility in saturation (μ) regime, using the saturation drain current expression $\{I_{ds(lin)} = \beta*[(V_g - V_{th})*V_{ds} - V_{ds}^2/2]\}$, where $\beta = (W/L)C_{ox}\mu$, and Cox is the dielectric capacitance. We found a channel mobility of 0.05, 0.3 and 0.03 $cm^2/(V\ s)$ for TFT's using SiO_2, SiO_xN_y and Si_3N_4 respectively. The highest value was obtained for the SiOxNy gate dielectric TFT, which probably is correlated with better insulator/a-Si:H interface properties, which at a time can be related with the lower mechanical stress associated with this film, as observed in previous works [12].

4. Conclusions

Bottom gate amorphous silicon hydrogenated based TFT's, with silicon dioxide SiO_2, SiO_xN_y and Si_3N_4 insulating layer and undoped amorphous silicon active layer were fabricated through a one deposition and one masking step process. A well-defined transistor action was obtained for all devices. We found the highest mobility for the silicon oxynitride gate insulator TFT, a result which can be related to the lower mechanical stress associated with this film leading to better insulator/a-Si:H interface properties.

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