

Weak-inversion topologies of analog median filters

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Design and implementation of two analog median filter cells are described. The first topology is a differential pairs array, which drain currents are driven into two nodes in a differential fashion. The second topology is based on a wide range OTA, which is used as basic block to maximize the dynamic range. Fabrication parameters for a MOSIS process of 1.6 μ m are used. Experimental results of two three-input fabricated prototypes are shown.

Palabras clave: Non-linear Filters; Median Filters; Weak-Inversion

1. Introduction

Nonlinear characteristics have made of median filters one of the most widely used in prefiltering applications for signal and image processing [1]. Since median filters are capable of remove impulsive noise and pixel dropouts, while the overall image quality is preserved, they have a great advantage over classical linear image processing. Despite their popularity, real-time digital implementations of median filters are computationally expensive [2, 3]. This is due to the fact that a sorting operation is required for each pixel. Since each element of data must be compared to the others, the circuitry needed to perform the median of a set of data is highly complex and very silicon area intensive.

Some works have been directed to reduce the number of data involved in the median computations [3], but parallel implementations of median filters using digital techniques are still not available. Another limitation of digital implementations of median filters is the fact that they are restrained to sequences that require double median computation, increasing hardware complexity. In recent research, some analog implementations of median filters have been reported [2-5]. Their simplicity has allowed some parallelism in image processing applications [6]. However, the most of these applications were based in bipolar transistors or MOS transistors working in the linear or saturation regions, and the total power consumption of those implementations sets a limit in the parallel capabilities of their applications.

The present work presents two implementations of median filters, with all the transistors working in the

subthreshold region. The very low power consumption of MOS transistors allows overcoming the power limitations for massive parallel processing implementations.

2. Circuit Description

The previously reported applications were based in bipolar transistors or MOS transistors working in the linear or saturation regions [4-6]. The total power consumption of those implementations sets a limit in the parallel capabilities of their applications. Analog circuits using subthreshold CMOS are of common use in applications with very low power consumption requirements [7]. Furthermore, since all the MOS transistors are operating in the limit of the weak-inversion region ($\sim 8\text{nA}$), their current gain is comparable to bipolar transistors; that fact allows the use of single-stage comparators to implement median filters with very low power consumption requirements [8].

The drain-source current in an NMOS transistor operating in the weak-inversion region is given by the equation [8]:

$$I_{DS} = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_{GB}}{U_t}\right) \left[\exp\left(\frac{-V_{SB}}{U_t}\right) - \exp\left(\frac{-V_{DB}}{U_t}\right) \right] \quad (1)$$

where V_{GB} is the gate to bulk voltage, V_{SB} is the source to bulk voltage, V_{DB} is the drain to bulk voltage, I_0 is the zero bias current, κ is the electrostatic source-drain coupling, and U_t is the thermal voltage. It can be observed some similarity with the Ebers-Moll equations, which can be

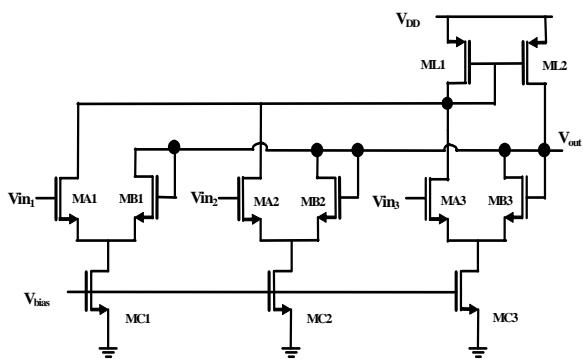


Figure 1. Differential pair-based median detector.

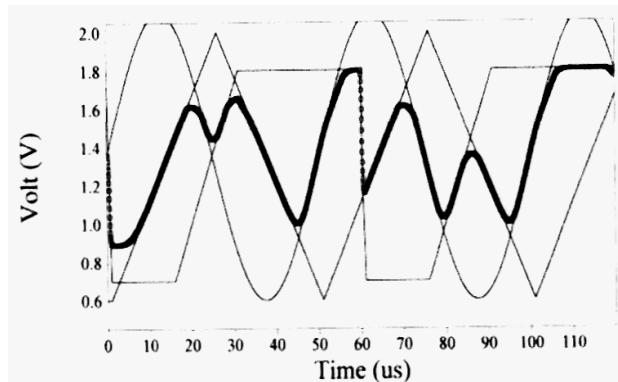


Figure 2. Performance of simulated three input median circuit.

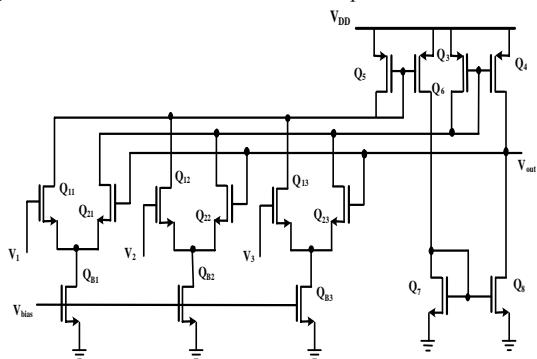


Figure 3. Wide band range median detector.

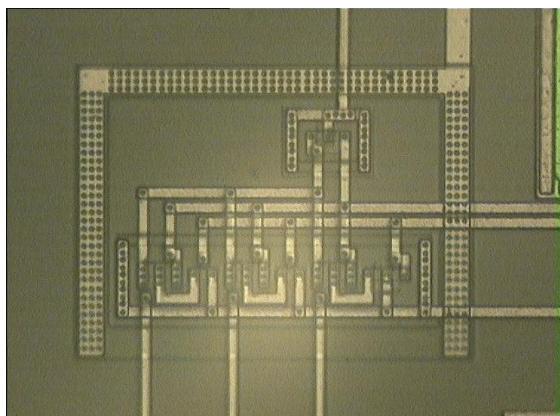


Figure 4. Microphotograph of the differential-pair based prototype.

explained because similar mechanisms are responsible of the current flow in both cases [9].

In a differential pair, if we assume $V_1 = V_{CM} + V_{DM}/2$ and $V_2 = V_{CM} - V_{DM}/2$ [7]:

$$I_{DM} = I_b \tanh\left(\frac{\kappa V_{DM}}{2 U_t}\right) \quad (2)$$

Figure 1 shows a median filter based on basic differential pairs, which transistors, M_{A1-A3} and M_{B1-B3} operate in subthreshold region, while M_{C1-C3} transistors are current sources controlled by voltage V_{bias} . Transistors M_{L1} and M_{L2} are used as active loads at figure 1.

A high current gain is obtained for small variations of the input voltage for V_{out} greater than 0.5 (saturation condition [7]). Since input signal is limited to a minimum of 0.5 volts, all six transistors will be in saturation.

During circuit operation, the output of the OTA's that can not follow the input will saturate in an alternate way, compensating these output saturation currents. Meanwhile, the other OTA will try to maintain the differences between the positive and negative inputs equal to zero, and that will maintain the median of the voltages at the output. Figure 2 shows the performance of a simulated three input median circuit.

3. Wide range median detector

Figure 3 shows a 3-input standard cell median, using a parallel structure [10]. In this approximation, the median filter is implemented using an extended-range amplifier [10]. Since a simple operational transconductance amplifier will not generate output voltages below V_{min} [8], the wide range amplifier uses two current mirrors to reflect the currents in the differential pair into the output node. Drain currents of Q_{11-13} are connected to the output through the current mirrors formed by Q_5-Q_6 and Q_7-Q_8 , while drain currents of Q_{21-23} are connected to the output using the current mirror Q_3-Q_4 . Since the output voltage has no effect on the input transistors, it has a range from V_{DD} to ground.

During circuit operation, the output of the input cells that can not follow the input will saturate in an alternate way, compensating these output saturation currents, while the other input cell will try to maintain the differences between the positive and negative inputs equal to zero, and that will maintain the median of the voltages at the output.

4. Results

A microphotography of the differential-pair based median filter fabricated prototype is shown in Figure 4. N-channel transistors have dimensions of $W= 8 \mu m$ and $L=5 \mu m$, and a bias currents of 3 nA. Figure 5 shows the experimental results.

Figure 6 shows the fabricated prototype of a wide range median detector, while Figure 7 shows the experimental results.

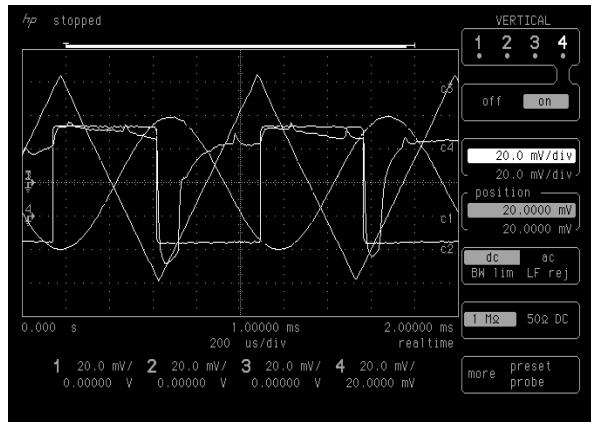


Figure 5. Experimental results of the differential-pair based prototype.

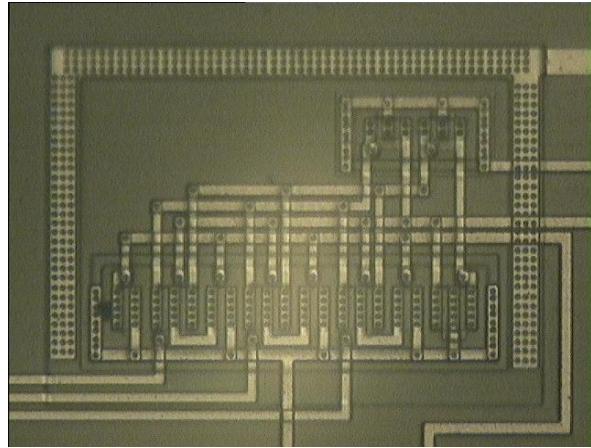


Figure 6. Fabricated prototype of a wide range median detector.

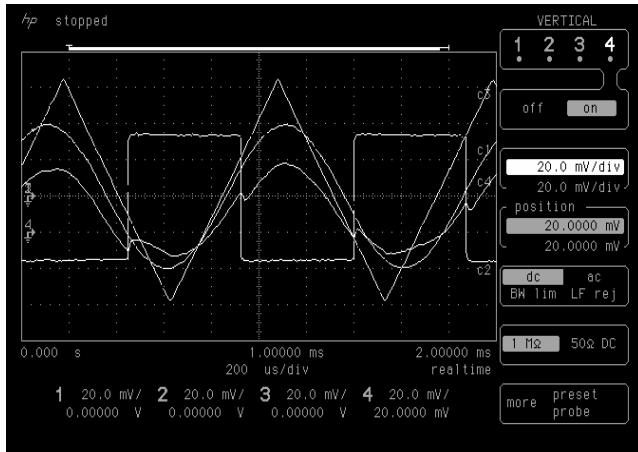


Figure 7. Experimental results of the wide range median detector.

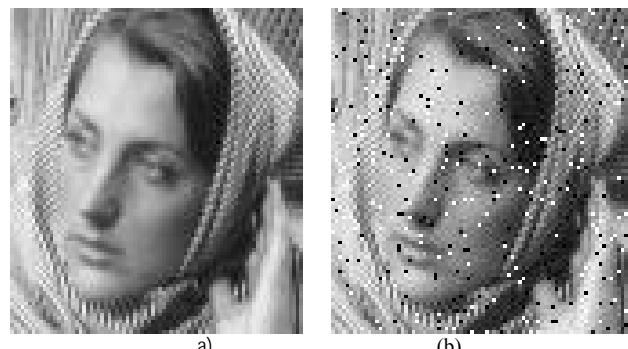


Figure 8. a). Original Image, b). Image corrupted with 15% salt and pepper noise, c). Reconstructed image.

Figure 8.b shows an image of 89 x 79 pixels corrupted with fifteen percent of additive impulsive noise. The range of the input signal will be from 0.25 volts to 1.15 volts, above the minimum voltage allowed. That input image is applied to an array of 88 x 78 basic median standard cell of 3 x 3 and the output is shown in figure 8.c. The total power consumption of the array will be less than 800 microwatts. The image was generated and corrupted using MATLAB®. A single 2.5 V voltage is used as power supply. The presented median filters operate with very low power consumption. For a 3 x 3 median filtering cell, the estimated total power is less than 80 nanowatts.

5. Conclusions

Two analog median filters, operating at the subthreshold region, have been described. Experimental results for three-input median detectors have been presented. The image filters have nine inputs, presented as a cell array of 3 x 3, and a single input. Simulated results demonstrate the feasibility of the approximation. The main characteristic of the systems is the very low power consumption of each cell. In addition, their simplicity will allow the massive implementation of median filters array for prefiltering applications. Since power consumption has been overcome, the possibility of using a median filter for each individual pixel in an image acquisition system is possible. The mean convergence time was around 2 microseconds. Despite the circuit's simplicity, the interconnection problem remains. Some masks with reduced neighborhood interconnection can be used to solve the problem.

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