Design of a JFET and radiation PIN detector integrated on a high resistivity silicon substrate using a high temperature process

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In this work, a fabrication process with a PIN diode integrated in a high resistivity silicon wafer is presented. This process uses high temperature thermal treatments to improve the JFET characteristics. Using simulation programs and statistical tools, the contribution of diverse process steps on the characteristics of the JFET manufactured in the same wafer with a PIN diode are evaluated. The use of thermal treatments has a significant impact on the JFET characteristics. The proposed JFET design offers an improved solution for the integration of JFETs on high resitivity silicon wafers.

Keywords: JFET; PIN; thermal treatments.

En este trabajo, se presenta un proceso de fabricación de un JFET con un diodo PIN integrado en una oblea de alta resistividad. Este proceso usa tratamientos térmicos de alta temperatura para mejorar las características del JFET. Usando programas de simulación y herramientas estadísticas, se evalúa la contribución de diversos pasos de proceso en las características del JFET fabricado en la misma oblea que un diodo PIN. Este proceso y diseño ofrecen una mejor solución para la integración de JFETs en obleas de silicio de alta resistividad.

Descriptores: JFET; PIN; tratamientos térmicos.

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1. Introduction

The technological process to fabricate PIN Diodes has remained the same since Kemmer and Holland [1,2] established the basic principles of production of these devices. Both authors avoid thermal treatments as much as possible, and because of this, it is difficult to integrate transistors and silicon PIN diodes on the same wafer [3,4]. These techniques produced high input capacitances, relatively low total gain and inadequate voltage isolation between the PIN high voltage bias and the JFET. In summary, these transistors do not have the same characteristics as discrete commercial JFETs that are normally used as preamplifiers. The reasons for these poor results are an excessively high channel doping, an abrupt channel-gate junction and a well that is not deep enough. These drawbacks could be improved using high temperature thermal treatments in order to have a better transistor doping profile. However this is in contradiction with the basic principles of these methods. Some works confront these arguments. In Ref. 5, 1100°C thermal treatments are used for 16 hours, to integrate transistors and PIN diodes, and [6] uses thermal treatments of 1200°C to obtain PIN diodes with dark currents in the range of 1-10 nA/cm^2.

Our own results show that two process steps are the key to minimizing the dark current: first to use an external gettering process, which should be the last high temperature treatment. The other important step is the cooling rate after the gettering anneal [7,8]. Cooling the wafers inside the oven at a rate of 25°C/hr until they reach at least 400°C has proven to be very effective. This allowed us to obtain PIN diodes with dark currents of 1-5 nA/cm^2 after thermal treatments of 1100°C and 1200°C for several hours. Our results show that, by using appropriate cleaning techniques and special care in the critical process steps, it is possible to use thermal treatments without markedly increasing the dark current of PIN diodes. Using this result in Ref. 9, a high temperature process to integrate a PIN diode and an improved JFET was proposed. In this paper a high temperature process to integrate a JFET and a PIN diode was analyzed by simulation, and the importance of appropriate thermal treatments in the JFETs characteristics is shown. This knowledge is then used to improve the process of the integrated JFET.

2. Technological Process

A 2kΩ-cm high resistivity substrate was used. Three implantations are used to form 3 different regions. The basic structure is shown in Fig. 1. After the B-implantation and thermal treatments, the P-Well concentration should be higher than 1×10^{15}cm^{-3} in the metallurgical junction of the P-well and the N+ channel. The channel N+ implantation defines the doping profile that determines the g_m and the C_j characteristics of the JFET and the appropriate relationship between them. The gate implantation is used to build the top gate, and its depth and width determine the capacitance and parasitic capacitances associated with the gate. The channel implantation and gate implantation were selected to obtain a pinch-off

TABLE I. Main JFET fabrication steps.

Process	Temp (°C)	Time (min.)	Dose (cm^{-2})
Initial oxidation	1100	180	
P+ Well Boron II, E=150 keV			2 E12
Oxidation	1200	180	
Inner thermal annealing	1200	120	
Oxidation	1100	180	
N+ Channel Phosphorus II, E=150 keV			1.5 E13
P+ PIN Boron II, E=120 keV			1.25 E 15
Oxidation	1100	120	
P+ Gate Boron II, E=80 keV			5 E 14
Oxidation	1100	30	
N+ Gettering Phosphorus II, E=120 keV			1.25 E13
Gettering	900	90	

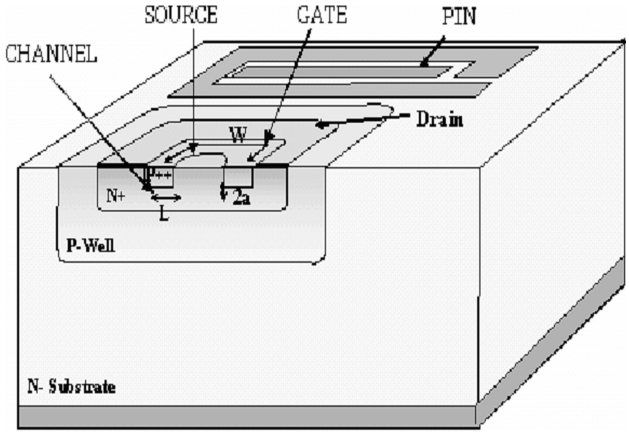

FIGURE 1. Schematic cross section of the integrated JFET and PIN proposed, (L= channel length, W gate width, 2a channel width).

voltage of 1 V. To limit the gate capacitance, a 5 μm gate maximum width was selected. The attainment of a low capacitance is necessary to fabricate a soft transition in the gate-channel junction. The latter can be done using an appropriate thermal treatment. The main process steps are shown in Table I.

All the thermal processes were selected according to Refs. 8 and 9 to avoid that the PIN leakage current increases beyond the desired range. It uses low energy implantations and long thermal treatments, with junction depths that make it possible to achieve a good g_m/C_j relationship. This parameter will be taken as a quality factor to evaluate the JFET performance. This process was simulated in ATHENA and ATLAS [Silvaco International]. The final impurity profile is shown in Fig. 2.

With these impurity profiles, a 9.6 μS/μm transconductance per unit length is predicted. A capacitance per unit of gate length of 2.48 fF/μm was obtained with the voltage

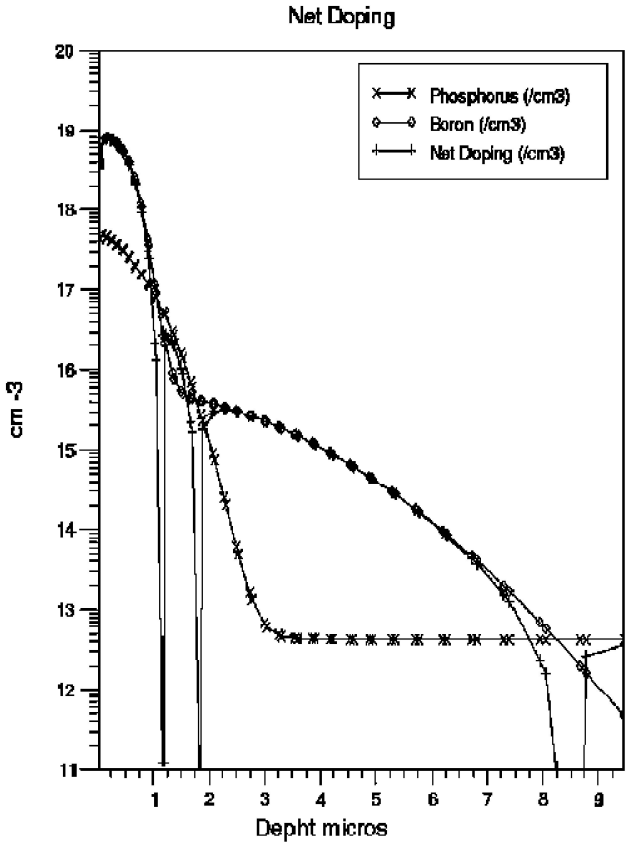

FIGURE 2. JFET doping profile concentrations.

gate-source forward bias [4,9]. Thus a value of 1.24 pF and 4.8 mS with a gate length of 500 μm is reached, and a g_m/C_j = 3.87 mS/pF. The value of the transconductance per unit length is similar to that reported previously [8]. However, this design offers a better capacitance-gain relationship comparable to commercial discrete JFETs. This improve-

TABLE II. Factors of the experiment.

Factors	Description
1	Initial oxidation
2	Well Boron implantation dose
3	Thermal annealing after 2
4	Channel Phosphorus implantation dose
5	Thermal annealing after 4
6	P+ Gate Boron implantation dose
7	Thermal annealing after 6

TABLE III. Result arrangement L8.

Exp.Num.	g_m (mS)	C_j (pF)	g_m/C_j
1	6.293	1.4	4.51
2	4.312	1.17	3.67
3	7.064	1.63	4.32
4	2.585	1.37	1.89
5	5.112	1.21	4.24
6	5.114	1.23	4.15
7	4.860	1.42	3.42
8	5.953	1.27	4.67

TABLE IV. Main effects g_m/C_j.

Factors	Level L1	Level L2	L2-L1
1	3.597	4.119	.521
2	4.142	3.575	-.568
3	4.067	3.65	-.418
4	4.122	3.595	-.527
5	4.412	3.304	**-1.109**
6	3.827	3.89	.063
7	3.492	4.224	**.732**

ment can be attributed primarily to the correct application of thermal treatments.

3. Analysis

To understand the effect of thermal treatments on the JFET characteristics, an orthogonal statistical study is proposed. The factors chosen in this study were the implantation dose of P+ well, N+ channel and P+ gate and the thermal treatments after these implantations used to soften the impurity profile of the transistor. These factors are shown in Table II.

The chosen levels are $\pm$ 10% of nominal dose or nominal time. In order to minimize the simulations to be carried out, an L8 factorial arrangement was chosen [10]. The results of the simulations are shown in Table III.

TABLE V. ANOVA g_m/C_j.

Fact	DoF	SS	F	Sum.	Per.
1	1	.546	69.929	.538	9.561
2	1	.644	92.493	.636	11.303
3	1	.348	44.648	.34	6.054
4	1	0.556	71.274	.548	9.747
5	1	2.453	314.17	2.445	**43.440**
6	1	.007	NC	NC	0
7	1	1.073	137.43	1.065	**18.925**
e	1	0.007			.97
Tot	7	5.629			100%

In all cases, appropriate voltage isolation exists up to 200 V. In order to analyze this result, the main effect method for evaluating the g_m/C_j was used [10]. Table IV shows that the greatest absolute values are produced by factors 7 and 5: thermal treatments made after the channel and gate implantations.

Factor 7 increases the depth of the gate-channel junction, improving the relation g_m/C_j, and factor 5 has the same effect. Factors 7 and 5 jointly produce a softer gate-channel junction. The statistical analyse recommend reducing the channel annealing time as much as possible, as stated by the sign of factor 5 in Table IV. The f-test of the experimental factors confirms that the thermal treatments are the main factors determining the variations of the transistor's performance (Table V).

Considering the results obtained and the sign of the main effects (Table IV and V), a confirmation simulation with these conditions was made, and C_j = 1.208 pF, gm = 6.184 mS, and g_m/C_j = 5.11 mS/pF were achieved. These results improve the g_m/C_j relationship of the device, and they are higher than those shown in our first simulated process (g_m/C_j = 3.87 mS/pF).

4. Conclusions

The relationship between gain and capacitance is strongly influenced by the doping profile of the JFET and can be improved using thermal treatments. Our results confirm than an adequate application of thermal treatments can improve the performance of JFETs on high resistivity silicon wafers, without altering the PIN leakage current.

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