Modelling the C-V characteristics of MOS capacitor on high resistivity silicon substrate for PIN photodetector applications

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This work proposes an electrical model to simulate the C-V measurements of the MOS capacitor on high resistivity silicon. High resistivity silicon is used as a substrate for PIN photo detectors. C-V MOS capacitor characteristics on high resistivity silicon substrates differ considerably from the C-V characteristics of low resistivity silicon substrates due to potential drop and majority and minority carrier response time. MOS C-V characteristics on high and low resistivity substrates at different frequencies were modelled by means of a series capacitor and resistor network. The system predicts the experimental results very well.

Keywords: MOS, HRS and LRS substrates; high and low frequency C-V characteristics; time of response majority and minority carriers.

Este trabajo propone un modelo eléctrico para simular las mediciones C-V del capacitor MOS en silicio de alta resistividad (SAR), el cual es usado como substrato para fotodetectores PIN. Las características C-V del capacitor MOS en SAR difieren considerablemente de las obtenidas en silicio de baja resistividad (SBR) debido a la caída de potencial y tiempo de respuesta de los portadores mayoritarios y minoritarios en el substrato. Las características C-V en substratos de SAR y SBR a diferentes frecuencias fueron modeladas mediante una red de capacitor y resistor en serie, la cual predice los resultados obtenidos experimentalmente.

Descriptores: MOS, substratos de silicio de alta y baja resistividad; características C-V en alta y baja frecuencia; tiempo de respuesta de portadores mayoritarios y minoritarios.

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1. Introduction

The C-V MOS capacitor characteristics give complete information about the semiconductor substrate and the oxide properties, so it is very desirable that this device should be the test structure for studying high resistivity silicon (HRS) substrates. However, MOS C-V characteristics on HRS are not simple to obtain compared to low resistivity silicon substrates (LRS). In other works, it has been shown that modelling the HRS substrate by a network of parallel resistor and capacitor is insufficient at high frequencies [1]. In the present work, the differences between the measured C-V MOS characteristics on HRS and LRS are analyzed, and their behaviour is modelled theoretically by a network of a series capacitor and resistor. The modelled outcome is completely in agreement with the experimental results even at high frequencies.

2. Experiment

SiO_2 films were thermally grown at an oxidation temperature of 1000°C in a gas mixture of O_2 (Oxygen) and TCE (Trichloroethylene). The substrates used were n-type (100) with LRS (2-2.6 Ω-cm) and HRS (2000-5000 Ω-cm and $>$ 4000 Ω-cm). Details about the experimental process can be seen in Refs. 2 and 3.

C-V measurements were done in low and high resistivity substrate MOS capacitors using a Keithley 595 Quasistatic C-V Meter at 1 Hz and a Keithley 590 C-V analyzer at 100 kHz. Results are shown in Figs. 2, 3 and 4. As expected, measurements at high frequency on devices with HRS show a reduced accumulation capacitance, C_o. This effect on C_o is even observed at higher frequencies (1 MHz), where the C_o measured is lower than the inversion capacitance. Furthermore, researchers could confuse the substrate type with these results.

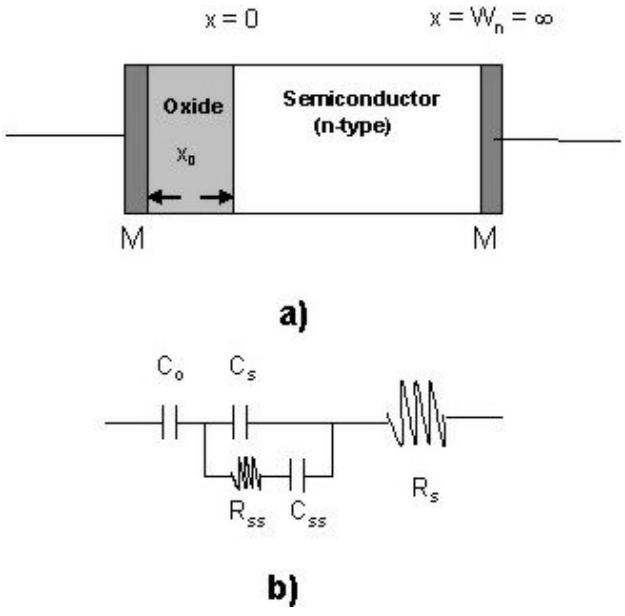

FIGURE 1. a) MOS capacitor structure, where M is the metal contact, and the substrate is n-type. b) MOS equivalent model proposed. R_{ss} and C_{ss} are the effective resistance and capacitance due to the surface states and interface trap density. R_s is considered when a high resistivity substrate is used.

3. Discussion

To understand why the C_o is not properly measured in an HRS, the following discussion is presented. Fig. 1a shows a sketch of the MOS structure with a semiconductor wafer of width W_n (thickness). In this device, the high frequency C-V measurement requires that

$$W_n \gg \sqrt{\frac{D_p}{\omega}}, \tag{1}$$

where D_p is the minority carrier diffusion coefficient, and ω is the frequency. If the frequency ω is $\gg D_p/W_n^2$, then the minority carriers cannot follow the high frequency signal [4]. In that case, the effective resistance and capacitance due to the combined effect of surface states and trapping centers (R_{ss}, C_{ss}) at the interface between silicon and silicon dioxide are neglected. Therefore, the high frequency condition

$$\omega_{ss} = \frac{1}{R_{ss}C_{ss}} \ll \omega, \tag{2}$$

is fulfilled and the total capacitance is

$$C_T = \left(\frac{C_oC_s}{C_o + C_s}\right), \tag{3}$$

where C_o is the oxide capacitance per unit area, and C_s is the capacitance of the semiconductor per unit area in high frequency [5]. Now, in Fig. 1b, considering the resistance of the HRS substrate (R_s) and the above mentioned condition, the total capacitance obtained is:

$$C_T = \frac{C_o\left[1 + \frac{C_o}{C_s}\right]}{\left[\left(1 + \frac{C_o}{C_s}\right)^2 + \left(\frac{\omega}{\omega_s}\right)^2\right]} \tag{4}$$

where $\omega_s = \frac{1}{R_sC_0}$. Equation (4) models the C-V MOS capacitor characteristics on HRS substrates as shows in the graphs of Figs. 2, 3, and 4.

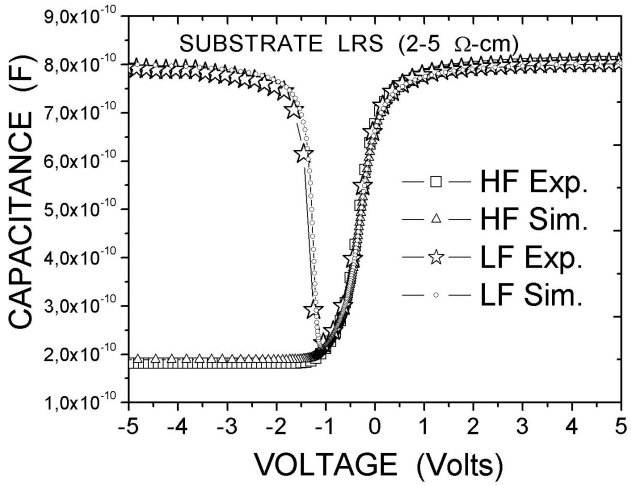

FIGURE 2. High and low frequency C-V curves, experimental and simulated, on low resistivity substrate (2-5 Ω-cm) with T_{ox}= 636 Å.

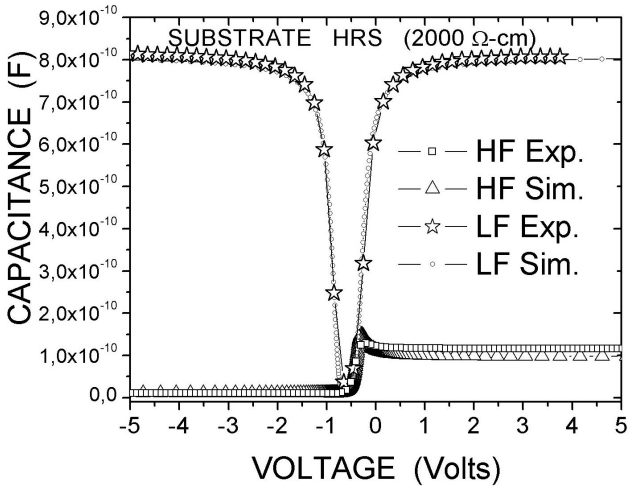

FIGURE 3. High and low frequency C-V curves, experimental and simulated, on high resistivity substrate (2000-5000 Ω-cm) with T_{ox}= 636 Å.

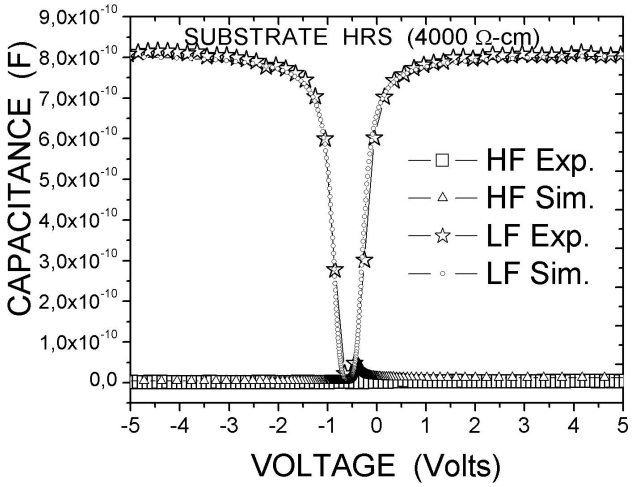

FIGURE 4. High and low frequency C-V curves, experimental and simulated, on high resistivity substrate (4000 Ω-cm) with T_{ox}= 636 Å.

The behaviour of the C-V curves at high frequency with HRS is related to the majority and minority carrier response time due to a variation in the high frequency voltage. Imagine a localized potential fluctuation of one thermal unit, k_0T/q, where k_0 is the Boltzmann constant, T is the temperature, and q is the electronic charge. This disturbance extends over a volume of radius about one Debye length, λ. The time for majority carriers to move a distance λ from the undisturbed environment to the center of the disturbance is the majority response time τ_{maj} [5];

$$\tau_{maj} = \frac{\lambda^2}{\mu(\frac{kT}{q})} = \frac{\varepsilon_s}{q\mu Nd} = \frac{\varepsilon_s}{\sigma}, \tag{5}$$

where μ is the mobility and σ is the conductivity of holes. Consequently, in a depleted NMOS capacitor biased in such a way that the surface is practically intrinsic the density of electrons is around 10^{10} cm^{-3},

τ_{maj}(interface) $\approx 0.5 \times 10^{-6}$ sec. near the depletion layer edge where n $\approx$ dopant density = N_d = 10^{15} cm^{-3} and τ_{maj}(depletion layer edge) $\approx 10^{-12}$ sec.

The response time, τ_R, for minority carriers in silicon at room temperature is typically 0.01-1 second in strong inversion; this response time is very long. For example, if $N_d = 10^{15}$ cm^{-3} and lifetime $\tau_{T=}10^{-6}$ sec., τ_R = 0.49 sec., this is very long as stated before. In the case of HRS, $N_d \approx 10^{12}$ cm^{-3}, then a τ_R= 0.73 μsec is obtained, which is very small compared to 0.49 sec. So the minority carriers respond much faster in HRS than in LRS and modify the behaviour of the C-V curves.

So, in our model, the R_s introduces a large RC constant those produces similar effects to that expected in HRS substrates. Using Eq. (4), it is possible to predict the C-V characteristics of MOS devices on HRS from low to high frequency. Moreover, the simulation done is able to replicate the lower accumulation capacitance compared to the inversion one. In the graphs of Figs. 2, 3, and 4, the simulated and the measured results are compared for 1 Hz and 100 kHz measuring frequencies. As can be seen, both curves match very well. Simulations at 1 MHz were also done and compared with results of Ref. 1; they also agree but are not shown here.

4. Conclusion

Modelling of the C-V characteristics at high and low frequencies on HRS and LRS substrates were done at different frequencies. A very good match with the experimental C-V curves was obtained from low to high frequencies in both HRS and LRS substrates. The C-V curves in HRS were modelled with Eq. (4) to predict the C-V curves at different substrate resistivities and different frequencies; both parameters can be varied easily. Simulations agree with experimental results from low to high frequency, and from low to high silicon resistivity substrates.

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