Computerized DLTS system to characterize deep levels in semiconductors

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A computerized system for deep level characterization in semiconductors has been set up. It is based on the well known DLTS (Deep Level Transient Spectroscopy) technique, but high versatility for data manipulation is achieved through an analog-to-digital conversion card (A/D) that digitizes capacitance transients. These transients are analyzed to provide information on the traps within the semiconductor. A PC-based program in Basic control acquisition, storage, analysis and presentation of results. The system is able of obtaining the desired parameters by only one temperature scan, which is an important advantage, taking into account the experimental time experimentally needed for the measurement. Experimental results for a silicon PIN power structure are shown, to illustrate its performance.

Keywords: DLTS; computerized; characterization

Se construy un sistema computarizado para caracterizar niveles profundos en semiconductores. Se basa en la bien conocida tcnica DLTS (Espectroscopa de Transitorios de Niveles Profundos), pero se obtiene gran versatilidad en el manejo de los datos porque usa una tarjeta de conversin analgico-digital (A/D) para digitalizar transitorios de capacitancia. Estos transitorios son analizados para obtener informacin de las trampas dentro del semiconductor. Una computadora personal controla la adquisicin, almacenamiento, anlisis y presentacin de los resultados de los datos. Se desarroll un programa en lenguaje Basic para alcanzar todos estos objetivos. Adems de su versatilidad, el sistema es capaz de obtener los parmetros deseados con solo un barrido en temperatura, lo cual es una ventaja importante en relacin con el tiempo necesario experimentalmente para realizar la medicin. Para ilustrar su funcionamiento, se muestran los resultados obtenidos para una estructura de potencia de silicio tipo PIN.

Descriptores: DLTS, computarizado, caracterizacin

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1. Introduction

Semiconductor devices have become very important components in most electronic equipment used in daily human activities. Their performance strongly depends on defects, which may be either desired or undesired. In any case, it is quite important to be aware of their nature and concentration in both, the raw and the processed material [1,2].

Defects can consist of impurity atoms within a crystal, point defects such as vacancies, interstitial atoms, or structural defects, such as dislocations and stacking faults [1,2]. The most important effects upon electrical parameters of electronic devices are both the minority carrier lifetime and the majority carrier mobility variations [3,4].

Several techniques have been developed to characterize semiconductor deep levels. Among them, we can mention Thermally Stimulated Capacitance (TSCAP) [5,6,7], and Thermally Stimulated Current (TSC) [8,9], which are specially useful for dielectric materials and high resistance semiconductors. Nevertheless, analysis of experimental data relies strongly on the precise value of the temperature rate of change used during the measurement and exhibit low sensibility. On the other hand, the Admittance Spectroscopy technique has evolved from the former capacitance and conductance measurements as a function of frequency and temperature [10,11]. Complete expressions for conductance and capacitance as a function of frequency have been derived [12,13] and former experimental results could be explained in terms of them. This is a specially useful method for narrow gap materials and low breakdown voltage devices but it is unable to characterize minority carrier traps. A more recent technique, DLTS (Deep Level Transient Spectroscopy), overcomes some of these drawbacks, becoming the most widely used technique for deep level characterization in many laboratories [14]. It is sensitive (detects trap concentrations about 10^{-4} times or less the concentration of shallow impurities in semiconductors), spectroscopic (exhibits a peak for each trap detected) and allows to obtain parameters from either minority (positive peak in the spectral result) or majority carrier traps (negative peak). Analysis of experimental information is direct and easy to interpret. This technique has become so important that nowadays, commercial systems can be found from several suppliers at more or less high prices. For obvious reasons, their performance can not be altered to pursue any additional benefit neither on software nor hardware. One advantage of setting up ours, is that different capabilities and components can be added as the set up requires them with the advantage of high flexibility. Furthermore, the algorithms used in any stage of the program can be redesigned at any time, changing any features of the system, at will, with a much lower price.

In Sec. 2, the equations necessary to develop the DLTS theory are shown. Then, the instrumentation of the system is explained in Sec. 3. Section 4 details the experimental results obtained and finally, the conclusion is included in Sec. 5.

2. The DLTS method

This method, takes advantage of either the current or capacitance transients produced by the thermal emission of carriers from the deep levels (also called traps) within the depletion region in a reversely biased diode, Schottky barrier or MOS structure. Such an emission process is produced by a sudden change of the negative bias value towards a more negative one. This is illustrated in Fig. 1 for the case of capacitance transients. In Fig. 1a the bias as a function of time is shown to change suddenly at time t_0 from a negative value V_1 down to a more negative value V_0. In Fig. 1b the energy band diagram of a Schottky barrier upon an N-type semiconductor with a deep level E_t is illustrated, with a depletion region width W_1, corresponding to a voltage V_1. Traps below the Fermi level are occupied by electrons. As this voltage is changed to V_0, the trend of the depletion region width is to increase, producing a stronger band bending, as shown in Fig. 1c. Hence, some of the traps first placed below the Fermi level E_f, are shifted up above E_f, increasing their probability of being empty. This means that an emission process, indicated by the heavy upward arrows in this figure, starts to take place. When released, electrons are swept out from the depletion region, due to the presence of electric field, producing the above mentioned current transient. At the same time, as they are released, electrons induce a charge change in this depletion region, leading to a capacitance transient shown in Fig. 1d. As time goes on, the capacitance tends to the value C_∞, corresponding to the steady voltage V_0.

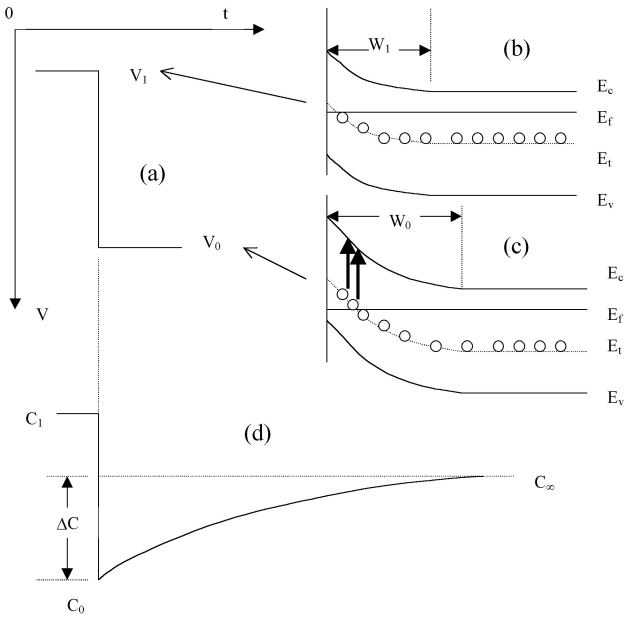

FIGURE 1. a) Bias change applied to either a diode, Schottky barrier or MOS structure to produce emptying of traps. The V_1 level corresponds to an electron filling pulse, V_0 to an emptying DC offset; b) Band bending prior and after changing bias, indicating the electron emission from deep levels shifted vertically above the Fermi level; c) Capacitance variation resulting from the charge exchange between traps and the conduction band.

The electron emission rate e_n towards the conduction band is given by the expression [3,15]:

$$e_n(T) = A\,T^2 \exp\left(-\frac{\Delta E}{kT}\right), \tag{1}$$

with

$$A = \frac{4\sqrt{6}\,\sigma\,k^2\pi^{3/2}m*}{h^3} \tag{2}$$

and T is the absolute temperature, ΔE the activation energy of the trap, k the Boltzmann constant, σ the trap cross section for electrons, m* the electron effective mass and h the Planck's constant. The temperature dependence of e_n in Eq. (1) is used to find values for ΔE and σ, which together with the trap concentration N_t completely characterize the corresponding deep level. Indeed, a semi-logarithmic plot of e_n/T^2 vs. 1000/T yields the above mentioned parameters from the slope and the y-axis intercept, respectively. Hence, all experimental methods are designed to provide the (T, e_n) pairs necessary to achieve such a plot.

In particular, the DLTS technique was designed to get the (T, e_n) pairs from either, current or capacitance transients. Only the case of capacitance transients will be discussed in this work. They can be written [15,16] as

$$C(e_n(T), t) = C_\infty + \Delta C\,\exp(-e_n t), \tag{3}$$

where ΔC is the transient amplitude and it is illustrated in Fig. 1d. It is related to the trap concentration by the approximate expression [15]

$$\frac{N_t}{N_d} = 2\frac{|\Delta C|}{C_\infty}, \tag{4}$$

which is valid whenever $N_t << N_d$.

In Fig. 1d, the case of a negative ΔC value is shown, which corresponds to emission from a majority carrier trap (electron trap in an N-type semiconductor). A minority carrier trap (hole trap in an N-type semiconductor) can be detected whenever minority carriers are injected to the depletion region. In P-N junctions this can be done by applying a positive bias V_1 to the sample. In this case, a positive ΔC value would be observed. When a Schottky barrier is used, minority carriers can not be injected by a positive bias, hence they should be injected by an alternative way, such as illumination. This fact allows extension of the DLTS method, arising the so called ODLTS (Optical Deep Level Transient Spectroscopy) technique [5].

The way in which the DLTS technique determines (T, e_n) pairs is by filling the traps with carriers, and then promoting emission. This is achieved by applying a pulse train involving both voltage values: V_1 and V_0 in Fig. 2a. At the same time, it changes the sample temperature and so induces the emission rate variation as shown in Fig. 2b. Then, an emission rate window is established by the system, in such a way that when the experimental emission rate traverses it due to

the temperature sweep (See Fig. 2c), the system provides an output signal extreme value (maximum for minority carrier traps or minimum for majority carrier traps), corresponding to a reference emission value (Fig. 2d). This value depends on the rate window and it is previously known. By repeating the thermal sweep with distinct rate windows each time, one can get several (T, e_n) pairs. The maximum height S_m of each peak in Fig. 2d is related to the transient amplitude ΔC by the expression

$$\Delta C = M\, S_m, \tag{5}$$

where the constant M depends on the precise characteristics of the system involved. For example, this procedure was first realized by using a Box-Car integrator [14] that samples transients at times t_1 and t_2 and yields the averaged difference C(t_1)-C(t_2) for several transients, as the output. Alternative ways to establish such rate window can be achieved by using either a Lock-In amplifier or an exponential correlator [17,18,15]. Either one performs a linear filtering function upon the train of capacitance transients, by using a corresponding weighting function w(t). The output S(e(T)), called the DLTS signal, is given as follows:

$$S(e(T)) = \frac{1}{T_0}\int_0^{T_0} C(e(T),t)w(t)\,dt, \tag{6}$$

where T_0 is the period of the train of capacitance transients. w(t) is the weighting function, that is determined by the specific instrument used as the filter. In this expression, the temperature dependence of both, the emission and the DLTS signal, is stressed because in the experimental setup, the output signal S(T) is plotted against the sample temperature for later analysis, as shown above in Fig. 2d. The most commonly discussed and used weighting functions are shown in Fig. 3. In Fig. 3a the original signal from a Box-Car integrator is shown. Fig. 3b shows the weighting function from a Lock-In amplifier and Fig. 3c corresponds to the weighting function as proposed by Miller *et al.* for an exponential correlator.

After experimenting with one of the above mentioned possibilities for setting up a DLTS system (the Lock-In mode) [15], we decided to set up a computerized digitizing system [19]. As explained before, the basis of this system consists of digitizing the capacitance transients produced by thermal emission, while the sample temperature is changed and measured. The above mentioned procedures to extract the trap information can also be used. Namely, linear filtering can be applied to these transients by numerical integration within the computer, to produce any desired correlation output. Then, the usual treatment can be done by analyzing the corresponding Arrhenius plot to get the activation energy and cross section of the trap. The concentration is calculated from the height of the corresponding peak by using the adequate relationship between S_m and ΔC. In fact, the Lock-In mode is again simulated in our program. This was first done

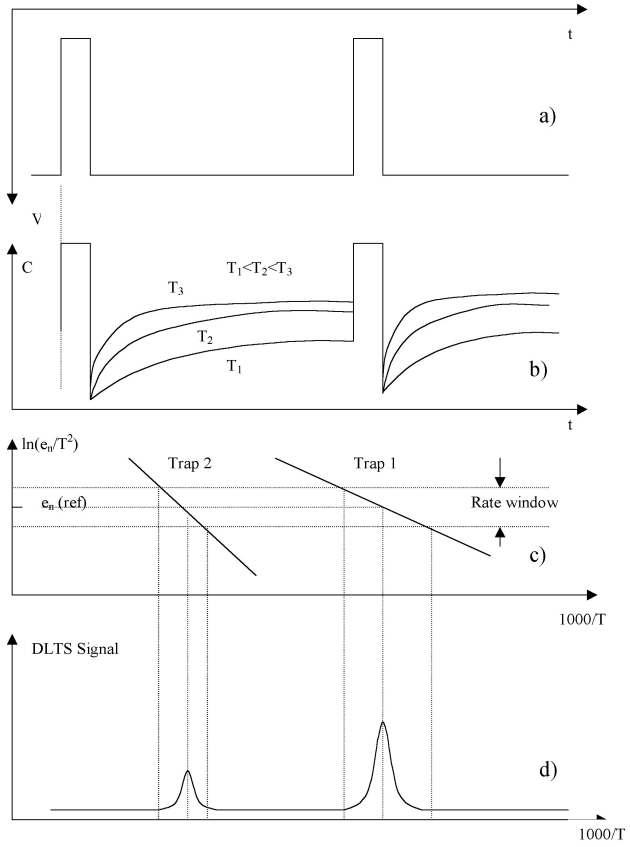

FIGURE 2. a) Voltage pulse train applied to the device under study to produce capacitance transients; b) Capacitance transients drawn for different temperatures; c) Arrhenius plot illustrating the meaning of the rate window, which is user pre-defined to establish a known emission rate at the DLTS signal peaks; d) DLTS signal showing some peaks ocurring within the pre-established rate window.

only for illustration purposes, but currently several correlation curves are calculated for the purpose of alternative analysis and comparison with results of the main algorithm.

The main algorithm used in our program is based on the idea proposed by Maguire and Marshall (M&M) [20]. Their method consists of analyzing each transient digitized to calculate its emission rate e_n (or e_p), amplitude ΔC and the capacitance C_∞ as t$\rightarrow\infty$. In this way, as the temperature is also recorded, each transient produces a point for the Arrhenius plot. Since each transient can be measured after less than 1 degree centigrade from the previous one, a great number of (T, e_n) pairs is potentially available for making the Arrhenius plot of each trap detected. An important point here is that all this information can be obtained with only one temperature scan, contrasting with traditional systems, which provide only one (T, e_n) pair with each different rate window (temperature scan) used.

In order to analyze the algorithm, the reader is referred to Fig. 4, where the main parameters considered are shown. In that figure, the time t_f corresponds to the net measurement time along the transient. Time zero corresponds to the tailing

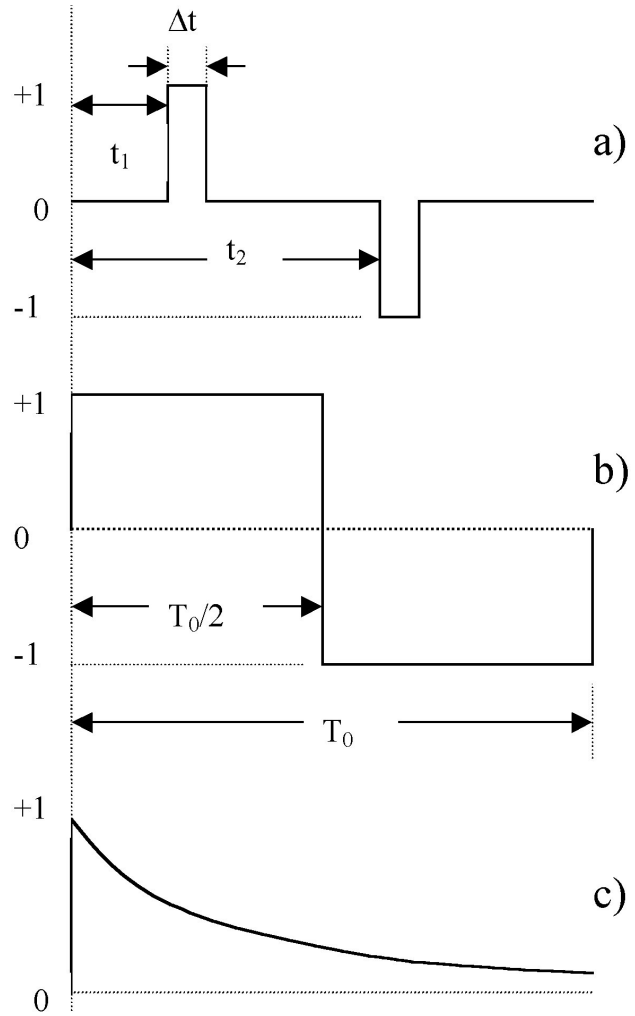

FIGURE 3. Different filtering functions used in traditional DLTS systems. a) The boxcar filtering function; b) The lock-in weighting function; c) The exponential correlation function.

edge of the trap filling pulse, but there is also a certain delay time t_d, after which the signal is numerically processed. In fact, the effect of this delay has been added to the original M&M method and was discussed by the authors formerly [22]. Also, a time t_i is defined in such a way that the horizontal line passing through the value $\overline{C}$ associated to t_i, determines two equal areas A and B in Fig. 4. As this time depends on the emission rate, calculation of t_i allows to determine e_n. In order to do this, it is seen that $\overline{C}$ can be calculated as

$$\overline{C} = \frac{1}{t_f - t_d}\int_{t_d}^{t_f} [C_\infty + \Delta C exp(-e_n t)]\, dt$$
$$= C_\infty - \frac{\Delta C}{e_n(t_f - t_d)}\left[exp(-e_n t_f) - exp(-e_n t_d)\right]. \quad (7)$$

Then, if this value is subtracted from C(t), it can be written as

$$C(t) - \overline{C} = \frac{\Delta C}{e_n(t_f - t_d)}\left[exp(-e_n t_f) - exp(-e_n t_d)\right]$$
$$+\Delta C exp(-e_n t). \quad (8)$$

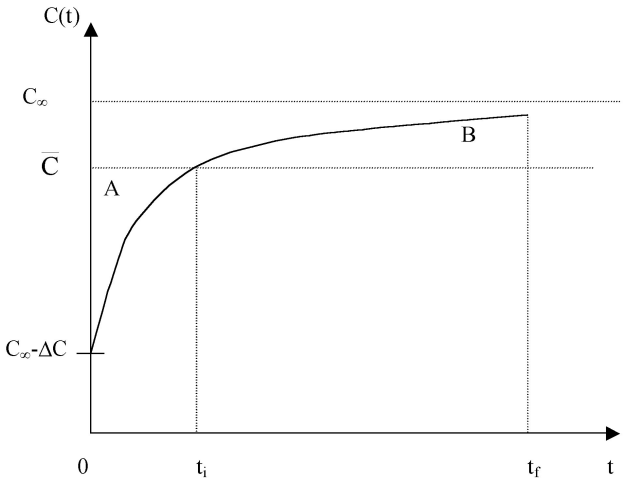

FIGURE 4. Basic concepts in the Maguire & Marshall method for transient analysis. Time t_i determines equal areas A and B along a measuring time t_f. Also shown is the capacitive transient amplitude ΔC.

In this way, C_∞ has been eliminated from these equations. At this point, it is important to notice that this last equation should be valid specifically for the time t_i. Hence:

$$0 = \frac{\Delta C}{e_n(t_f - t_d)}\left[exp(-e_n t_f) - exp(-e_n t_d)\right]$$
$$+\Delta C exp(-e_n t_i) \quad (9)$$

or, equivalently,

$$e_n(t_f - t_d)exp(-e_n t_i) = exp(-e_n t_d)$$
$$-exp(-e_n t_f). \quad (10)$$

This equation implies that whenever t_i t_d and t_f are already known, then e_n can be numerically calculated.

According to the expressions presented above, the next procedure is applied to analyze each transient acquired by the A/D conversion card:

a) Calculation of $\overline{C}$ by using numerical integration of the (t_i, C_i) pairs (Currently, Simpson's rule is used for this task).

b) Determination of the t_i value corresponding to $\overline{C}$. (This is done by direct comparison of $\overline{C}$ with each C_i value. If there is no agreement, linear interpolation is used to get a better approximation).

c) As the times t_d and t_f are already known, Eq. (10) can be numerically solved for e_n. At this stage, Newton's method is used. At this point, a (T_i, e_{ni}) pair is available for the Arrhenius plot that will provide the activation energy ΔE and cross section σ.

By using the emission rate value e_n calculated in (c), Eq. (3) should be valid for each time-capacitance experimental pair along the corresponding transient. Hence, it can be written as

$$C_j = C_\infty + \Delta C \, \exp\left(-e_n t_j\right). \tag{11}$$

In order to use the information provided by all the points measured along the transient, an equation with C_∞ and ΔC as unknowns $_\infty\Delta$can be constructed by summing up for all these points:

$$\sum_j C_j = N \, C_\infty + \Delta C \, \sum_j \exp\left(-e_n t_j\right), \tag{12}$$

where N is the number of points in the summation. As another equation is required, it can be constructed by multiplying Eq. (11) by t_j and then summing again:

$$\sum_j C_j t_j = C_\infty \sum_j t_j + \Delta C \sum_{t_j} \exp\left(-e_n t_j\right). \tag{13}$$

Then, Eq. (12) and (13) are easily solved for the unknowns C_∞ and ΔC. With these values, Eq. (4) is used to calculate the relative trap concentration N_t/N_d. This last proposal to calculate trap concentration was also added by the authors to the original M&M method [21].

The above outlined method is represented in the block diagram shown in Fig. 5.

3. The experimental setup

The functions described above can be done by the experimental setup shown in Fig. 6. A brief description for the function of each part can be given as follows: the sample is introduced in a cryostat that permits to sweep the sample temperature from near 77 K up to about 425 K; the pulse generator provides the train of pulses that, throughout the capacitance meter, fills with electrons some traps in the space charge region; the capacitance meter measures the capacitance transients of the sample; the oscilloscope allows to view both, the train of pulses and also the capacitance transients produced; these capacitance transients are fed through a signal conditioning amplifier into an A/D conversion card, which provides the digitized data to the computer. At the same time, temperature is also controlled and digitized by the temperature controller and then it is acquired by the computer through a GPIB IEEE-488 interface; the TTL output of the pulse generator is used, through a connection card, to synchronize the start of transient digitizing.

A DT2801 Data Translation board was used, where analog to digital (A/D) and digital to analog (D/A) conversions can be performed, as well as digital input and digital output transfers. Programming can be done with interpreted or compiled BASIC language. Software packages as PCLAB and PCTHERM can be used also. Some important characteristics of the DT2804 board are summarized:

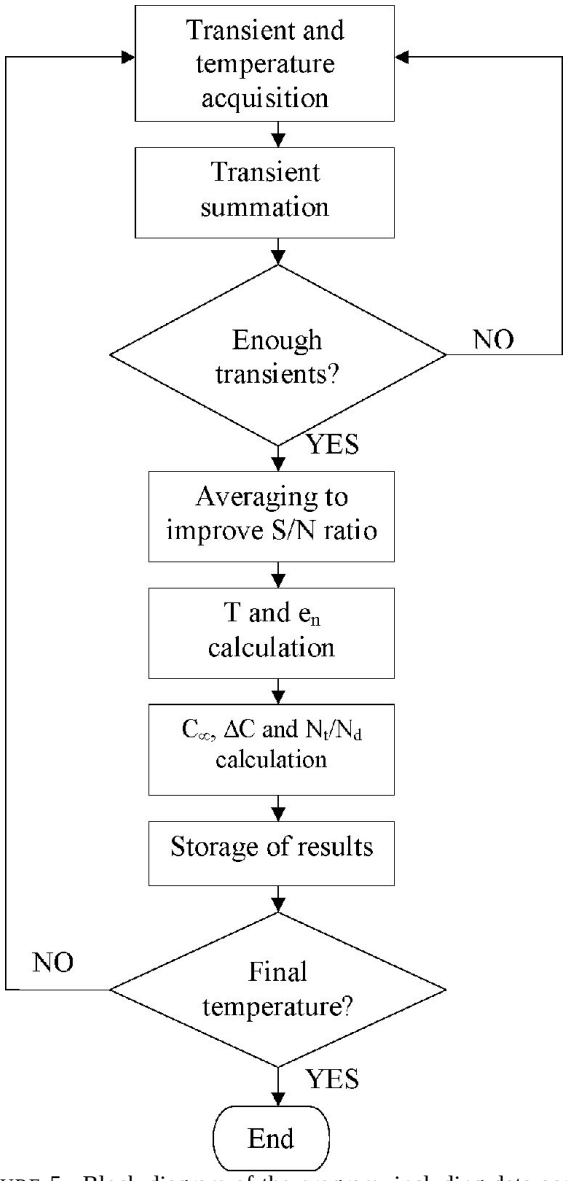

FIGURE 5. Block diagram of the program, including data acquisition, basic parameter calculation for further analysis and result storage until the temperature scan is completed.

- Resolution: 12 bits.
- Number of analog inputs: 16 single ended, 8 differential input.
- Software programmable gain range: 1, 2, 4 or 8.
- A/D throughput to system memory: 13700 samples per second.

Operation of the board can be user configured with internal jumpers. Currently, the configuration selected for our measurement system is A/D 0-10 V unipolar differential mode input. As the A/D conversion card was provided with some assembler language routines ready to be called from a Basic language program, the whole program was written in GWBASIC language.

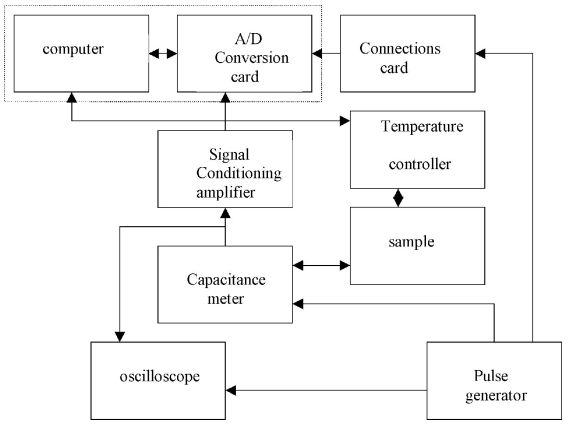

FIGURE 6. DLTS system schematic, indicating with arrows the information flow.

The program structure is shown in Fig. 7 in a block representation. As seen, after variable definition and initialization, two main menus are defined by using the pre-definable keys of the computer. Menu no. 1 is to enter data, from either a previously acquired and stored file (F1), or from direct measurement of a sample (F2); when this key is pressed, another menu to establish the measurement conditions is displayed; after these conditions are entered, the temperature scan can be started. When data are available in the computer memory, the F3 key allows to transfer control to menu no. 2. Within this menu one can make an Arrhenius plot (F1) in order to recognize the distinct straight segments defined by the experimental points, each one corresponding to one defect. Then, calculations proceed by selecting the appropriate sets of aligned points (F2) (user defined) to perform a least squares fitting of each set. The straight line fitted is plotted upon the experimental points for comparison. According to the above mentioned theory, at this stage a value for each of the parameters defining the defect, is calculated. Then, a plot of relative concentration for the different defects observed is also drawn (F3). Straight lines representing the values calculated before are also superimposed to assess the fitting accuracy. After calculations for the various defects observed have been done, a table of these results can be obtained (F5). Also, a capacitance (C_∞)-temperature plot can be drawn (F7). Finally, a set of four correlation signals (Lock-In type) simulated from the same transients for different rate windows can be plotted (F9); this can be useful for both illustrative reference and to perform an alternative calculation as used formerly in the original method.

4. Experimental results

In order to show how the system works, a PIN diode made in our laboratory without ahy special gettering process was measured from near room temperature down to about -80 ˚C. The results that will be presented, were obtained by scanning temperature at a time rate under about 8 ˚C/min for most circumstances (in some cases was less than 6 ˚C/min). This ensured data reproducibility by avoiding thermal delays. Sampling was done along three different times: t_f= 197, 97 and 49 ms, using a filling pulse train with periods $T_0 \sim 225\ ms$; $\sim 120\ ms$ and $\sim 65\ ms$, respectively. In all cases, sampling was done each 1 ms. Also, 1 ms (T_d) was deleted from the beginning of the capacitance transient. The filling pulse width was 1 ms. The PIN diode was biased with a -10 V offset and pulses of 12.5 volts height superimposed in order to assess the possible detection of minority carrier traps.

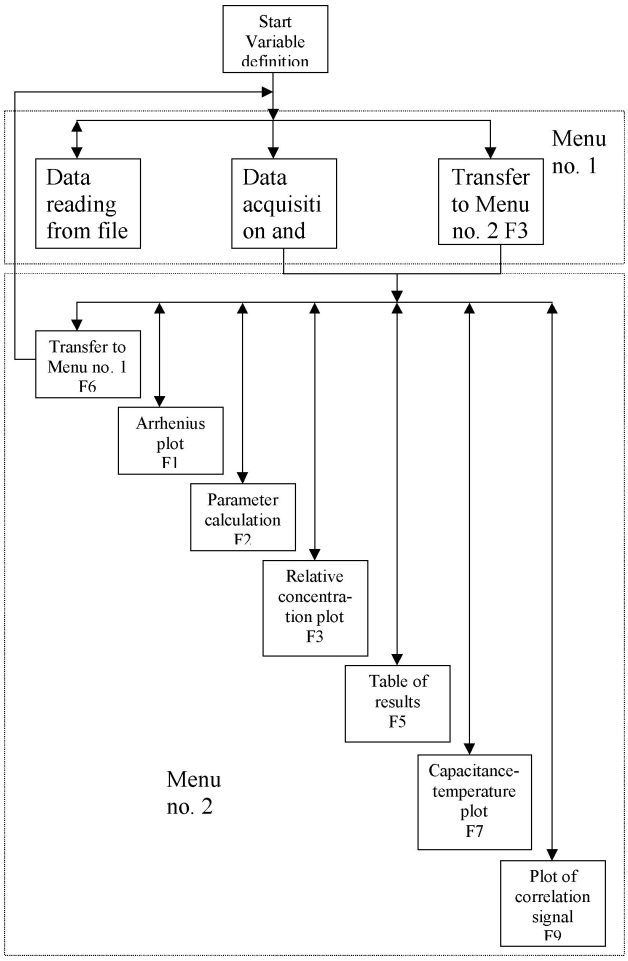

FIGURE 7. Practical structure of the complete program, including those parts designed for the complete analysis of the stored data during acquisition.

Data were recorded under both, cooling and heating cycles to confirm that no thermal delay existed. This can be seen in Fig. 8, where the Lock-In correlation signals from six thermal scans appear; two (cooling and heating) for each t_f value mentioned above. As seen, there is no appreciable delay between the heating and cooling curves. One negative peak is clearly visible, as a result of emission from a certain trap. The emission rate in the peak depends on the sampling time mentioned above (t_f) and the deleted time ($t_d = 1\ ms$). The explicit relationship is shown in Table 1. The effect of moving the rate window to higher emission rates is seen as a peak shift toward higher temperature. This is in agreement

with Fig. 2c. At lower temperatures, another negative peak starts to grow, but it is not completely traced as the scan was stopped near 190 K. Because they are negative, both are ascribed to majority carrier traps (electron traps in this case). As said before, in the traditional DLTS analysis this information is the basis of the method, because the temperature of each peak is experimentally available along with its corresponding emission rate. It is clear that in such kind of analysis, partial peaks as that appearing at low temperature in Fig. 8 would not be useful at all. Hence, to attain the necessary information, the thermal scan should be extended down to lower temperatures if possible, in order to complete the second peak for the DLTS spectrum. In our system, each one of the points plotted provides both, the temperature and the corresponding emission rate, if this is placed within the system detection limits. Hence, in case that this condition is met, such a point provides information for the Arrhenius plot. Our system is able to measure emission rates within an approximate range from $\sim 1 s^{-1}$ up to ~ 2000 s^{-1}. The lower limit is defined by the longest time sampled along the transient, which is related to the specific capability of the digitizing card, program and computer used to acquire and process efficiently an increasingly amount of data. Instead, the higher limit is determined by the capability of the system to sample with a high rate (high sampling speed of the digitizing card and short response time of the capacitance meter are needed); also, the noise level of the system is expected to affect such upper limit. The above mentioned range corresponds to 1 ms sampling times along ~ 800 ms of the transient.

In Fig. 9, the Arrhenius plots corresponding to the heating cycles in Fig. 8, are shown. There are defined two straight lines with negative slope, each one composed of three superimposed segments, one corresponding to t_f= 197 ms (squares), the second to 97 ms (circles) and the last to 49 ms (triangles). Clearly, as seen for the defect (no. 1) placed at higher temperature (lower 1000/T), the lines for different t_f do not span the same emission rate range, because shorter t_f's fail in measuring low emission values. Anyway, in the range where they superimpose, a good agreement is found. The parameters extracted from the analysis of the Arrhenius plot for the case of t_f= 197 ms when heating, are shown in Table II for both defects detected. Defect 1 could be associated to divacancies [22] and defect 2 to the so-called E center in silicon [23] (this is a phosphorus-vacancy pair). Also shown in table 2 are the relative concentrations calculated from Fig. 10a in the range where the results form an approx-

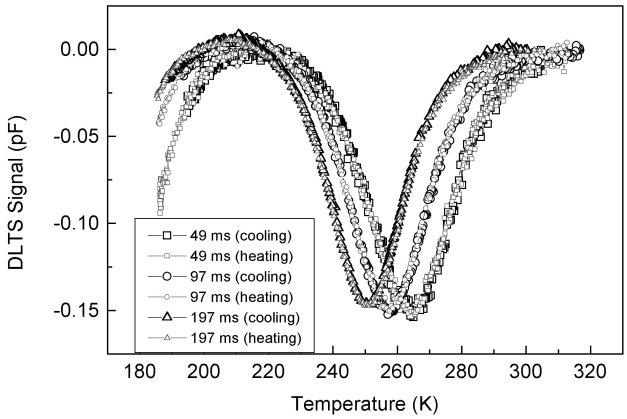

FIGURE 8. An example of DLTS signal simulation (Lock-In type). There are six curves for three rate windows: two temperature scans for each one. A good agreement between the cooling and heating cycles can be seen.

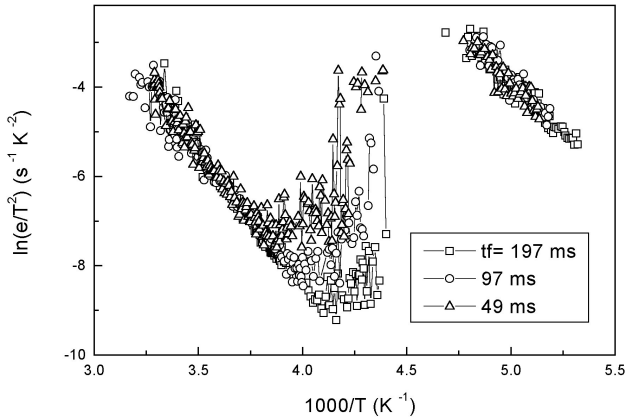

FIGURE 9. Arrhenius plots for the heating cycles shown in Fig. 8. The different emission span seen is associated to the low capability to extract low emission rates with shorter times of data analysis. Nevertheless, where the plots are superimposed, the agreement is good.

TABLE I. Specific values for the parameters M in expression (5) and the emission rate in the peak maxima for the DLTS spectra in Fig. 8. They were calculated for a deleted time t_d= 1 ms.

t_f (ms)	M	e_m (s^{-1})
197	0.201	12.6
97	0.198	25.3
49	0.194	49.0
21	0.181	108.4
9	0.156	227.1
5	0.128	362.6

TABLE II. Activation energy, capture cross section and relative concentration calculated with the DLTS system and program, for both defects detected during the partial temperature scanning performed.

Parameter	Defect 1	Defect 2
$\Delta E(eV)$	0.534 ± 0.005	0.421 ± 0.011
$\sigma(cm^2)$	$(1.21 \pm 0.31) \times 10^{-14}$	$(8.94 \pm 5.81) \times 10^{-13}$
N_t/N_d	$(3.5 \pm 0.5) \times 10^{-2}$	$(3.7 \pm 1) \times 10^{-2}$

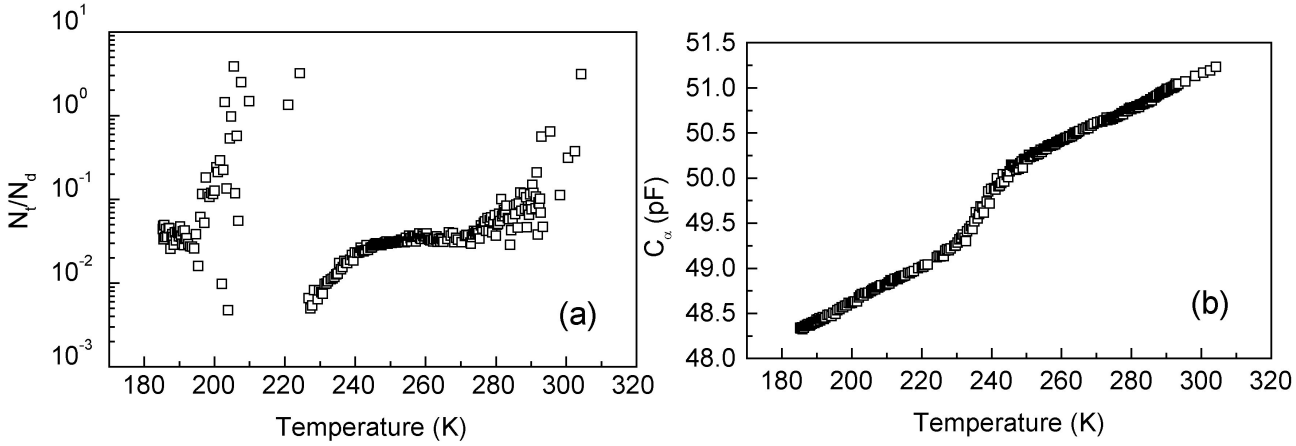

FIGURE 10. a) Relative concentration calculated with expression (4). The values reported in table 2 correspond to an average in the range where the plots are nearly horizontal; b) Capacitance C_∞ as a function of the temperature. The step-like change can be ascribed to the charge exchange produced by the defect 1.

imately horizontal line. Assuming Nd $\approx 10^{14}$ cm^{-3}, such relative concentrations yield absolute trap concentrations of $(3.5 \pm 0.5) \times 10^{12}$ cm^{-3} and $(3.7 \pm 1) \times 10^{12}$ cm^{-3} for the defects 1 and 2, respectively. The capacitance C_∞ appearing in equation 3 and illustrated in Fig. 5 is also calculated for each point in the experimental data. Such values appear in Fig. 10b. This plot represents the temperature variation of the capacitance for a fixed bias (the V_0 level in Fig. 1; -10 V in our case). The step-like increase (about 1 p height) of the capacitance between T $\approx$ 222 K and $T \approx 250$ K, is attributed to the rapid emptying of defect 1 and could also be related to the trap parameters under a proper analysis similar to that used for thermally stimulated capacitance. As seen, a small increase of the sample capacitance about 3 pF is produced by the thermal scan in the temperature range from $\sim$180 K to $\sim$310 K.

5. Conclusion

A versatile computerized DLTS system has been setup in our laboratory, with the possibility of enhancing both hardware and software, at a much lower cost than commercial systems. The structure and working frame have been demonstrated by using a PIN diode. The algorithm introduced by Maguire and Marshall was enhanced by the authors. One advantage of the algorithm used, is that results can be obtained with simple calculations and only one temperature scan, contrasting with the classical technique. On the other hand, other types of signal processing, such as Fourier and Laplace analysis can be settled up in the same hardware. This would be useful in attempting to resolve several traps which are emitting in the same temperature range. This is part of our future work with the system.

1. M. Lannoo, J. Bourgoin, *Point Defects in Semiconductors* (Vol. 1), *Theoretical Aspects* (Springer-Verlag, Berlin, 1981).
2. S.K. Ghandhi, *Semiconductor Power Devices* (John Wiley and Sons, New York, 1977).
3. J.P. McKelvey, *Solid State and Semiconductor Physics* (Harper and Row, New York, 1966).
4. D.K. Schroder, *Semiconductor Material and Device Characterization* (John Wiley & Sons, Inc., New York, 1990).
5. P. Blood and J.W. Orton, *The Electrical Characterization of Semiconductors: Majority Carriers and Electron States* (Academic Press, London, 1992).
6. L.R. Weisberg and H. Schade, *J. Appl. Phys.* **39** (1968) 5149.
7. J.C. Carballes and J. Lebailly, *Solid State Commun.* **6** (1968) 167.
8. M.C. Driver and G.T. Wright, *Proc. Phys. Soc.* (*London*) **81** (1963) 141.
9. M.G. Buehler, *Sol. St. Electron*. **15** (1972) 69.
10. C.T. Sah and V. C. K. Reddi, *IEEE Trans. ED*-**11** (1964) 345.
11. L. Forbes and C.T. Sah, *IEEE Trans. ED*-**16** (1969) 1036.
12. W.G. Oldham and S. S. Naik, *Sol. St. Electron.* **15** (1972) 1085.
13. C. Ghezzi, *Appl. Phys. A* **26** (1981) 191.
14. D.V. Lang, *J. Appl. Phys.* **45** (1974) 3023.
15. A. Avila, *Caracterización de niveles profundos en semiconductores mediante la técnica de DLTS*, Tesis de Maestría, CINVESTAV del I.P.N., Dep. de Ingeniería Eléctrica (SEES), México, D. F., 1983.
16. M. Lannoo, and J. Bourgoin, *Point Defects in Semiconductors* (Vol. 2), Experimental Aspects, (Springer-Verlag, Berlin, 1981).
17. G.L. Miller, J.V. Ramirez and D.A.H. Robinson, *J. Appl. Phys.* **46** (1975) 2638.
18. D.S. Day, M.Y. Tsai, G.B. Streetman and D.V. Lang, *J. Appl. Phys.* **50** (1979) 5093.

19. A. Avila, A. Reyes, A. Escobosa, *Sistema de DLTS basado en el uso de una tarjeta de conversión analógico-digital (A/D)*, Informe Técnico no. 123, Serie Amarilla, Centro de Investigación y Estudios Avanzados del I. P. N., Departamento de Ingeniería Eléctrica (SEES), México, (junio de 1992).

20. H.G. Maguire and A. Marshall, *IEEE Trans on Instr. And Meas.* **IM-35** (3) (1986) 313.

21. A. Avila G., A. Reyes B., *IEEE Trans. on Instr. and Meas.* **43(6)** (1994) 936.

22. A.H. Kalma and J.C. Corelly, *Phys. Rev*. **173** (1968) 734.

23. J.W. Chen and A.G. Milnes, *Ann. Rev. Mater. Sci*. **10** (1980) 157.