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Developing Micro-Columns of Test Sockets to Enable Processor Validation Signals

Desarrollo de Micro-Columnas de Sockets de Pruebas para Habilitar Señales de Validación del Procesador

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Technological Innovation: Electrically Conductive Material Characterization and Optimization.

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Resumen

Este estudio aborda el desafío de optimizar la interconexión entre procesadores y micro almohadillas de contacto (uADC) durante el proceso de validación. Se busca aprovechar las señales de depuración para medir y diagnosticar interfaces en los procesadores, utilizando un interposer de depuración como interfaz de medición. Las uADCs representan una alternativa para incorporar contactos adicionales en la validación al ocupar un espacio entre las almohadillas del procesador comercial. Sin embargo, su desarrollo enfrenta desafíos tecnológicos como la reducción del área de contacto y la estabilidad de resistencia eléctrica. Para abordar estos desafíos, se propone el uso de un socket de interconexión (SDI) con tecnología de micro columnas de interconexión (uCDI), capaz de cumplir con la conductividad requerida. Los resultados experimentales muestran mediciones de resistividad eléctrica por debajo de cien ohmios, el cual es el valor máximo aceptado dentro del contexto de validación de procesadores. La implementación de las uADC y el uso del SDI con uCDI ofrecen ventajas en el proceso de validación al proporcionar acceso a señales previamente inaccesibles, sentando un precedente para futuras investigaciones en la miniaturización de contactos en productos comerciales.

Palabras clave: micro almohadillas de contacto, procesador, interposer depuración, Sockets de interconexión, micro columnas de interconexión.

Abstract

This study addresses the challenge of optimizing the interconnection between processors and micro contact pads (uADC) during the validation process. The aim is to leverage debug signals to measure and diagnose interfaces in the processors, using a debug interposer as a measurement interface. The uADCs represent an alternative for incorporating additional contacts in validation by occupying a space between commercial processor pads. However, the development of uADCs faces technological challenges such as reducing the contact area and ensuring electrical resistance stability. To address these challenges, the use of an inter-connection socket (SDI) with micro–column interconnect (uCDI) technology, capable of meeting the required conductivity, is proposed. Experimental results demonstrate electrical resistivity measurements below one hundred ohms which is the maximum accepted value within the context of processor validation. The implementation of uADCs and the use of SDI with uCDI offer advantages in the processor validation process by providing access to previously inaccessible signals**,** setting a precedent for future research in contact miniaturization in commercial products.

Keywords: micro contact pads, processor, debug interposer, interconnect socket, interconnection microcolumns.

1. Introduction

Microprocessor's developers often use product reference platforms to execute the validation of the IC packages. A reference platform consists of a Printed Circuit Board (PCB) which is equivalent to a commercial board, but is fully equipped with all available Input/Output modules [1].

In addition, there is an interposer board and a Land Grid Array (LGA) socket which sits on top of the reference platform [2]. This socket is made up of leaf springs contacts that are soldered to the PCB on the bottom side, and on the top side they connect to the interposer pads. To connect the interposer and the Integrated Circuit (IC) package, a burn-in socket is used which usually consists of flexible elastomer-based electrical interconnect columns with gold particles incrusted inside the elastomer [3] [4]. This socket is disposed on top of the interposer board to add the capability of fast exchange for the IC package connected to the interposer [5] [6].

In many cases, the LGA patterns of the ICs have a unique pitch dimension; consequently, the burn-in socket requirement is linked to this individual pitch and the physical dimensions of pads. Nevertheless, by introducing the use of Micro Pad technology [5] in IC packaging, new demands emerge with respect to the state-of-the-art, which include the mixture of Pads and uPads in the whole grid array pattern. To cope with the problems caused by multi-pads, one of the challenges presented is the reduction of the pitch between the different pads. To solve the physical space problem, the uPad size was reduced, to the point that the uPad can be placed in between the regular Pads without any potential interference, this solution was developed and patented [7] with the title "Framework including an interposer having an atypical shape".

The usage of uPads, on the other hand, presents new challenges for the performance of the burn-in socket columns [6], which will interconnect the newcomer IC uPads [8] [9]. The signal integrity performance of the columns represents an additional complexity,

as reducing the column volume, raises the risk of increasing resistivity in the electrical interconnection [10]. This resistivity must not exceed one hundred milliohms to be suitable for the testing environment.

The objective of this study is to develop innovative socket micro columns (uColumns) within the burn-in testing environment. The primary goal is to enable efficient interconnection between the micro signals of the processor during the validation phase. By incorporating these interconnections, the study aims to enhance the reliability of the processors and improve their overall performance.

As depicted in Figure 1. Interconnection system components, the composition of the assembly is formed by an IC package 1 that is placed on the top of the whole assembly. The IC package is constructed by a die 7, which is a small block of semiconductor material, finally, on top, an integrated heat spreader 6 (IHS) is attached over the die.

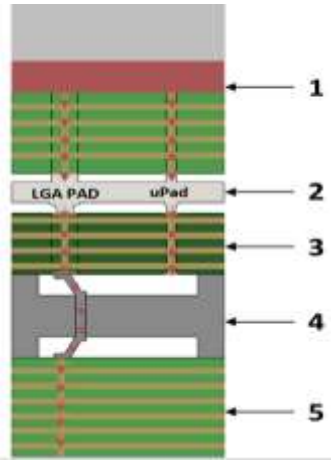

Figure 1. Interconnection system components.

[11] Located on the bottom of the die, there is a ground grid array 9, that connects the Flame-Retardant Level 4 (FR4) substrate 10 using a thin layer of copper, to connect the latest uPad 8, additionally, layers receive the signals from the die, and then a plated vias 11 connects the top Pads with the bottom LGA pad 13 and the bottom uPad on package 12.

Underneath the IC package, a Burn-in socket 2 is placed. This socket consists of an elastomer 16 that connects the different elements in the socket. One of those elements is the LGA Contacts 14, 15, which connect to the bottom LGA pads of the IC package. On the other hand, there are other contacts on the bottom of the socket. These contacts are like the ones located on top 19, 20, and their function is to connect the socket and the substrate 3 board.

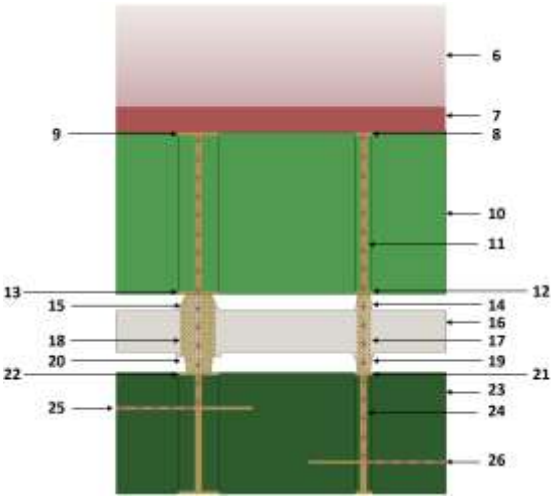

Figure 2. Interconnection subsystem components.

The uColumn 17, 18 [11] conduct the signals between the socket´s top and bottom contacts. These columns are made of gold particles encrusted into an elastomer material, as shown in Figure 3. Burn-in socket columns.

Figure 3. Burn-in socket columns.

The burn-in socket is disposed on the top face of an Interposer 3, using LGA pads 21, 22 located on top of a printed circuit board FR4 23. These pads are connected through the board with the help of copper vias 24. These vias are subsequently routed through the different layers on the PCB, further inter-connecting to the PCB surface of the interposer and other sections 26 with the LGA pads 26. The rest of the components in the system are the LGA Socket 4 and Reference Platform 5.

The main difference between LGA columns and uColumn is the physical dimension. LGA columns diameter is 0.35mm**,** while the diameter of the uColumn is 0.15mm. As a result, the total volume is reduced, hence the density is also reduced. The columns required a total compression of 0.1mm to be activated, Figure 4. Socket column diagram, shows this behavior, before and after the columns are compressed. To accomplish the desired compression, the legacy force per column is 25 +/- 10 grams.

Figure 4. Socket column diagram.

Validation platforms are typically evaluated according to the product specification of temperature ranges from -40 ℃ to 120 ℃. As the temperature change, different effects occur in the columns. One of the effects that have a greater impact is the thermal expansion of the elastomer of the gold particle impact tapping column.

Figure 5. Effect of boundary conditions, shows the socket in an uncompressed state, the gold particles 27 contacts 29 among them is marginal having a high resistance. Figure 5. Effect of boundary conditions, shown a compression of 0.1mm at an ambient temperature of ~24℃; with this contraction the gold particles have contact between them, consequence increasing the electrical conductivity through the column.

Nevertheless, when the temperature rises in the system up to 120℃, the golden particles separate following the elastomer 28 expansion caused by its thermal properties; hence, the electrical resistivity increases through the columns.

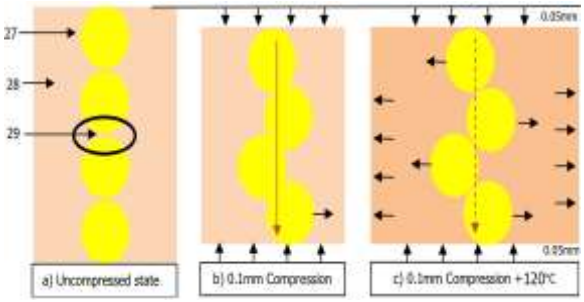

Figure 5. Effect of boundary conditions.

This study is characterizing the LGA Columns and the uColumn relationship between the compression of the column and the electrical conductivity through it within a high-temperature environment.

The described invention [7] [11] introduces an innovative system designed to interconnect small signals on an integrated circuit (IC) and provide access to those signals using an interposer. While the specific details of how the IC and interposer micro signals are interconnected are not covered, this article draws inspiration from the described invention. It conducts a thorough study of the challenges involved in achieving electrical interconnection and proposes a solution tailored to this application.

By addressing the challenges associated with interconnecting small signals on ICs, the proposed solution aims to enhance signal integrity, minimize noise interference, and optimize space utilization. It recognizes the importance of efficient access to these signals and acknowledges the limitations of conventional methods. Building upon the foundation laid by the described by the invention described above, this article proposes a novel approach that promises to revolutionize the interconnection process.

The proposed solution, although not explicitly detailed, is the result of careful analysis and consideration of the unique demands posed by small signals interconnections. By leveraging the capabilities of an interposer, the system seeks to bridge the gap between the IC and the external connections, facilitating easier access to the signals while ensuring reliable and robust electrical interconnection. While further details are needed for the proposed solution, this article offers valuable guidance for future research and development in this fields.

2. Materials and Equipment

The socket columns are developed by the company ISC® [6], the composition of this material is an elastomer [12] [13] and gold particles are incrusted as shown in Figure 3. Burn-in socket columns. Figure 6. Uniaxial test data shows the stress/strain chart of the hyperplastic material characterized using a five-term Moodley-Rivlin in Ansys® [14].

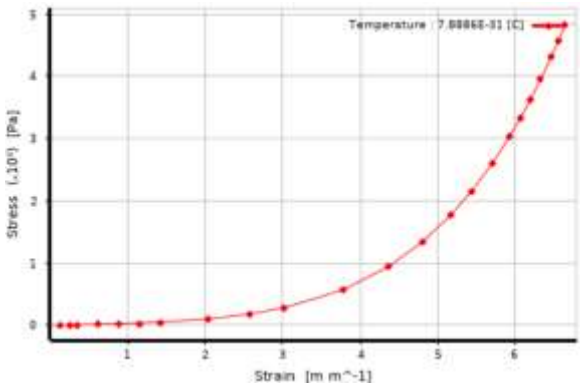

Figure 6. Uniaxial test data.

Due to the material´s incompressibility, the function can be as shown in the equation:

$$W = W_D(\bar{I}_1, \bar{I}_2) + W_b(J) \quad \textbf{(Eq. 1)}$$

Where $W_b(J)$ represents the volumetric strain energy function and J the Jacobian and $W_D(\bar{I}_1, \bar{I}_2)$ the deviatoric strain energy function. The polynomial is based on the first variant deformation $\bar{I}_1$ and the second variant deformation $\bar{I}_2$ of the Cauchy-Green tensor [15].

$$W = \sum_{i+j=1}^{N} C_{ij}(\bar{I}_1 - 3)^j + \sum_{K=1}^{N} \frac{1}{d_k}(J - 1)^{2k} \quad \textbf{(Eq. 2)}$$

Where C_{ij} and d_k are required in the model. For the five-terms:

$$W = C_{10}(\bar{I}_1 - 3) + C_{01}(\bar{I}_2 - 3) + C_{20}(\bar{I}_1 - 3)^2 + C_{11}(\bar{I}_1 - 3)(\bar{I}_2 - 3) + C_{02}(\bar{I}_2 - 3)^2 + \frac{1}{D_1}(J - 1)^2 \quad \textbf{(Eq. 3)}$$

Another phenomenon that is governing the model is the effect of the thermal expansion of the material due to the presence of thermal loads in the system. Thermal expansion can be described as the change in shape, area, volume, and density in response to a change in temperature. The coefficient of thermal expansions on nanocomposites is defined as [16]:

$$\beta = \frac{1}{V}\left(\frac{\delta\rho}{\delta T}\right)_P \quad \textbf{(Eq. 4)}$$

Where β is the coefficient of thermal expansion, where V is the volume, T is the temperature and P is the pressure in the system. In terms of density the equation can be represented as:

$$\beta\ (T) = \frac{-1}{\rho}\left(\frac{\delta\rho}{\delta T}\right)_P \qquad \textbf{(Eq. 5)}$$

3. Experimental Methods

The experimentation was conducted using a lab experiment, a simulation, and a correlation between both. The lab experiment includes five different devices to emulate the system function. Additionally, the characterization of the boundary conditions that emulate the system environmental aging; includes the controlled temperature and loading, and the required instruments to measure the behavior on two columns as shown in Figure 7. Testing set-up.

Figure 7. Testing set-up.

One of the test devices is a test vehicle that was made to mimic the IC package's physical dimensions including the LGA pads and uPads 29. uPads are connected in groups, as shown in Figure 8, which allows measuring of the electrical resistance on a test board.

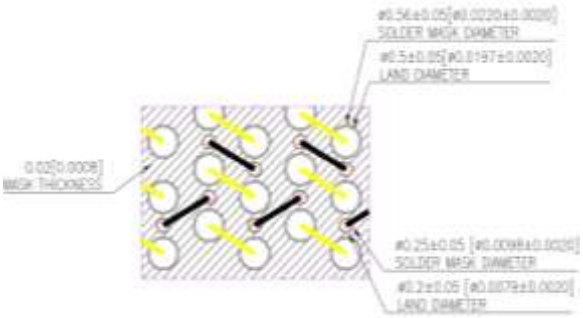

Figure 8. Test vehicle land pattern.

The second device is a functional Burn-in Socket [6] developed with the LGA columns and uColumns 28. The third device is a test board that mimics the function of the interposer [11] 27. When both devices are connected then the daisy chain is closed. The test board is shown in Figure 9. Test board land pattern. The fourth and fifth devices are a Legacy LGA socket and a legacy reference platform.

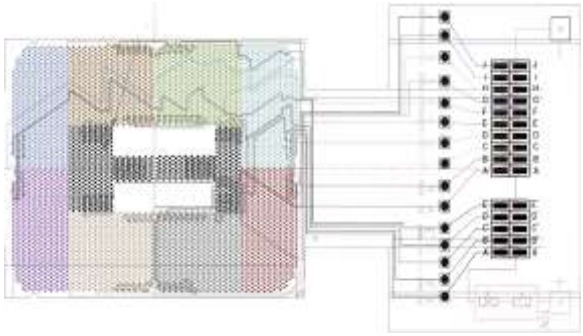

Figure 9. Test board land pattern.

To control this load, a retention mechanism 30 was designed to apply load using a back plate support that keeps the reference board stiff and on the top side [17], a heatsink applies the load to the system using linear compression springs, as shown in Figure 7. Testing set-up. This load was calculated to apply a total force of 25 grams per column. This force is calculated with the formula:

$$F = k\ (\ x - \ x_0\ ) \qquad \textbf{(Eq. 6)}$$

Where k represents the spring constant and x the system in equilibrium and x_0 the compression of the spring.

This study is aiming to evaluate the novel uColumns by performing laboratory testing and simulation processes to understand the conductivity that should be X<100uΩ. The analyzed material has been characterized to calculate the amount of resistance that passes through it, by plotting the compression and the reaction force after the compression.

To collect readings of the resistance in the system, during the test experiment, a data logger DATAQ INSTRUMENTS® model DI-245, was attached to a digital multimeter AGILENT® Model HP 34401A was connected to the interposer test board surface mounted connected to the testing pads. With this interconnection, it was possible to access to the diverse groups of daisy chain signals. The system was analyzed using different temperature boundary conditions from -40 ℃, 25 ℃, and 120 ℃. A Thermotron® S/SM series environmental thermal chamber was used to create a profile oscillating between the lowest and heights temperature. Measurement was recorded every 30 seconds for a period of 48 hours.

A finite element analysis (FEA) was conducted using the simulation software ANSYS® [14]. A model was created using the information from the Socket builder [6], as well as the IC and interposer specifications. Figure 6. Uniaxial test data depicts the different elements in the model; The study is a two bi-dimensional analysis, with an axisymmetric graphical expansion used as axial. Figure 10. Test board land pattern shows the section on contact representation.

The interposer pad is represented by the letter A, this pad is fixed and connected to the column with a frictional contact of a friction coefficient of 0.2; on the other side, the IC pad is represented by the letter B, this pad has a displacement on the -Y axis of 0.1mm and connected to the column with a contact with a coefficient of friction of 0.2. both pads have material of cooper and are connected to the column with frictional contact.

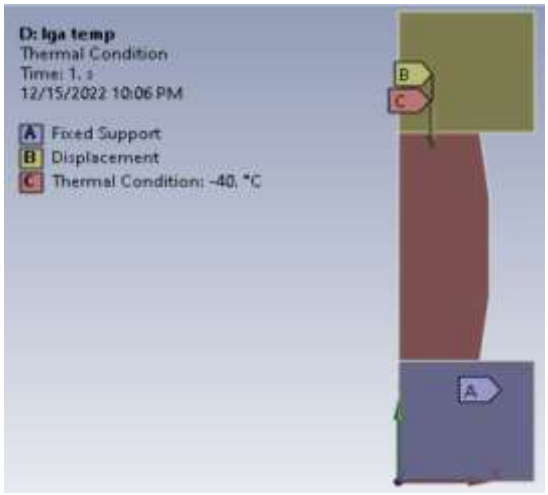

Figure 10. Test board land pattern.

4. Results

By finding the reaction force at certain compression, this result can be correlated to the column characterization graph shown in Figure 11. Column characterization Resistivity/Force graph. Where it can be observed the behavior of the column compression and the force at different temperatures. The Resistance is also plotted on the right.

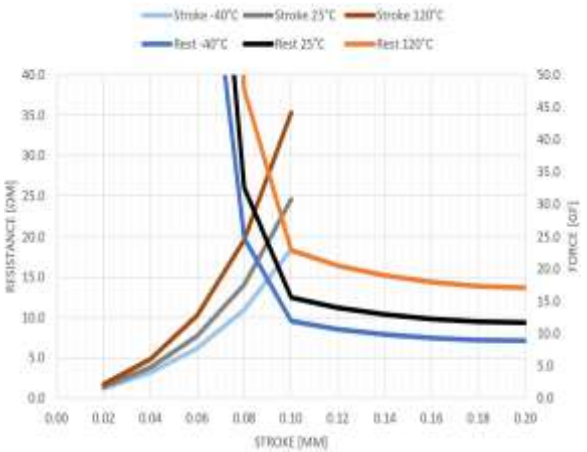

Figure 11. Column characterization Resistivity/Force graph.

A similar graph for the uColumn is shown in Figure 12. uColumn characterization Resistivity/Force graph. As the dimension of the column changes the behavior also changes.

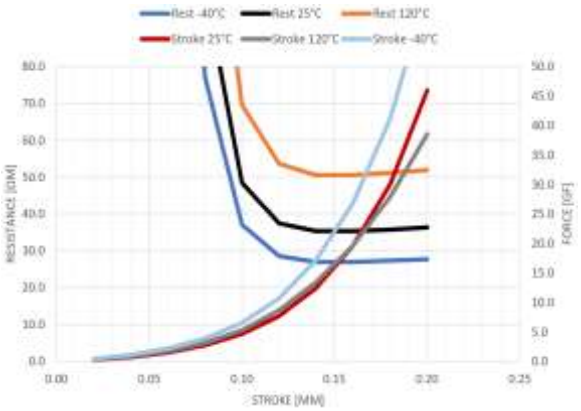

Figure 12. uColumn characterization Resistivity/Force graph.

The measurements in the labs are depicted in Figure 13. Test measurements. Two different lines are plotted; the orange line represents the measurement of the LGA columns. While the uColumns are represented with a blue color. The resistance [18] [19] oscillates as the temperature changes over time. When the system reaches the temperature of 120°C. The measurement of the uColumns, after the resistance stabilization, is 63.2 mΩ. For the LGA Columns, the measurement is 24 mΩ. this is caused due to the deformation that occurred on the material.

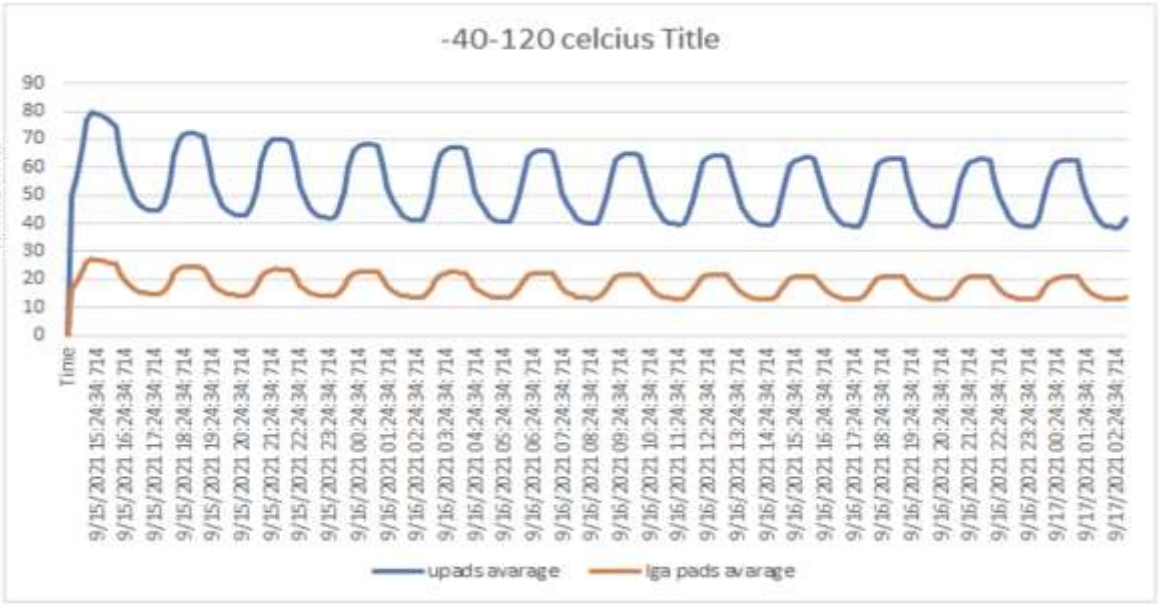

Figure 13. Test measurements.

To have a better understanding of the material behavior three different scenarios are shown; as a baseline, it was modeled the current LGA column at 120°C and a total compression of 0.1mm, Figure 14. LGA Column Deformation, shows the LGA pad deformation with a maximum deformation of 0.0309mm.

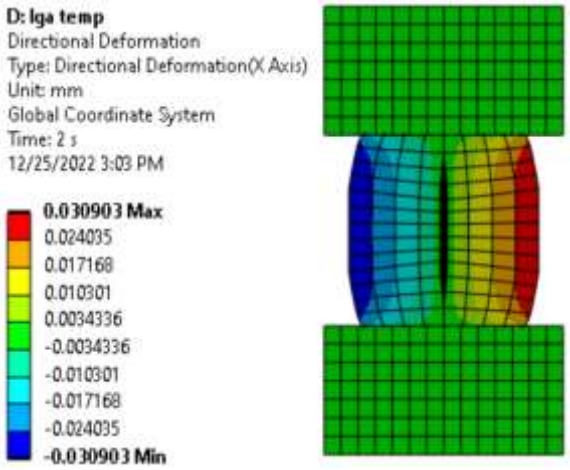

Figure 14. LGA Column Deformation.

Figure 15. LGA Column Force/Deformation depicts the relation of the deformation within the compression, the behavior is linear, and is correlated to the thermal strain. On the other side, the reaction force is a curve, and it is equivalent to the equivalent stress, the force when the stroke reaches 0.1mm is ~35 gf.

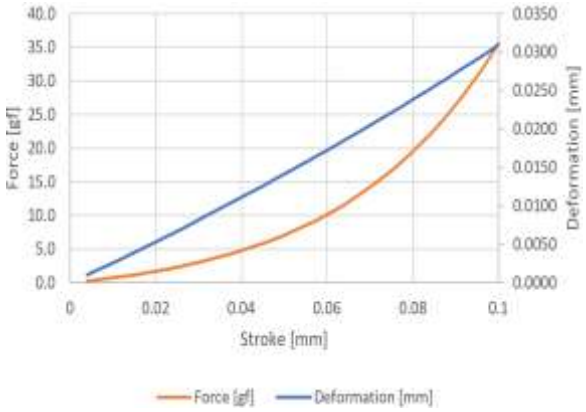

Figure 15. LGA Column Force/Deformation.

The uColumn simulation shows a smaller deformation, of only 0.0175mm at a compression of 0.1mm, the reason is due to the reduction of the volume itself.

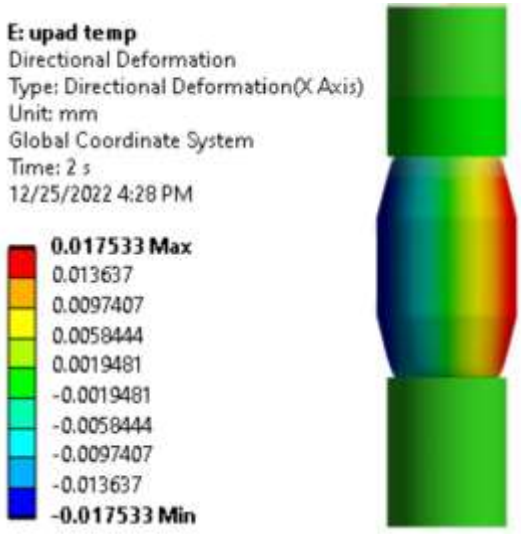

Figure 16. uColumn Deformation.

As the deformation also decreases the reaction force is also decreasing. Figure 16. uColumn Deformation shows the behavior of the force which is as low as ~11gf.

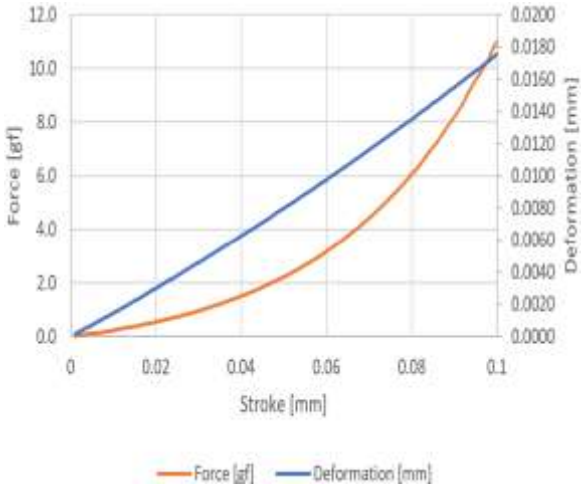

Figure 17. uColumn Force/Deformation.

The correlation factor in shown Figure 17. uColumn Force/Deformation allows to know the resistivity in the column, and iteration was run to evaluate the resistivity at different temperatures. Figure 18. uColumn Resistance/Temperature depicts the resistance behavior [20] [21]

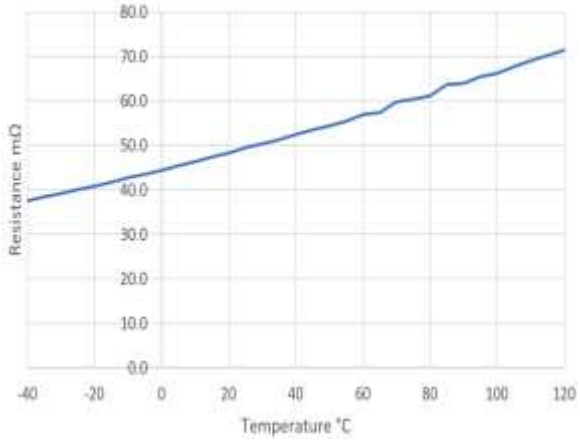

Figure 18. uColumn Resistance/Temperature.

Table 1. Simulation results presents the results for various scenarios at higher temperatures, incorporating an additional stroke of 0.14mm. The LGA Column at 120°C is 22.9 mΩ, and the resistance increases when the uColumn is characterized, to 69.5 mΩ. When the stroke increases from 0.1mm to 0.14mm to the same uColumn the electrical resistance decreases to 23.0 mΩ.

Table 1. Simulation results.

Temperature (°C)	Stroke (mm)	Force (gf)	Resistance (mΩ)
COLUMN			
-40	0.1	18.3	**11.9**
25	0.1	24.0	**15.6**
120	0.1	35.2	**22.9**
uCOLUMN			
-40	0.1	5.7	**37**
25	0.1	7.5	**48.5**
120	0.1	10.7	**69.5**
uCOLUMN with 0.14 mm STROKE			
-40	0.14	15.0	**15.0**
25	0.14	18.2	**18.2**
120	0.14	23.0	**23.0**

The correlation between the FEA model with the measured data in the lab is shown in Figure 19. Column FEA vs Measured, in Figure 20. uColumn FEA vs Measured the values are close to each other especially at low temperatures, in the temperature of 120°C de delta is slightly larger, but the margins stay closed.

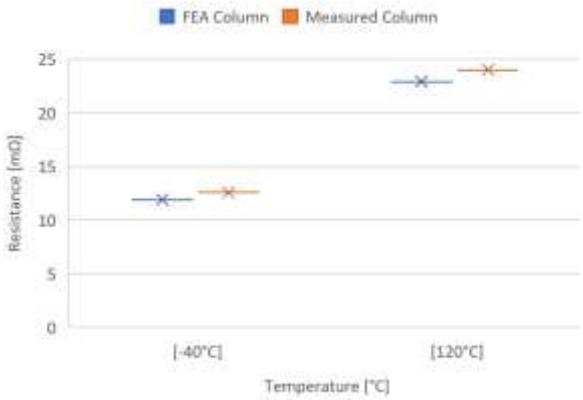

Figure 19. Column FEA vs Measured.

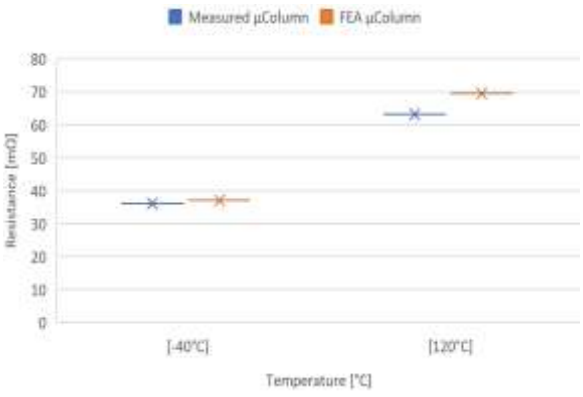

Figure 20. uColumn FEA vs Measured.

5. Conclusions

The research conducted in this study presents compelling evidence that the uColumns integrated into the SDI are highly appropriate for Burn-in applications. The obtained resistivity values fall significantly below the critical threshold of one hundred milliohms, making them well-suited for use in debug applications as well.

Moreover, the study goes beyond the assessment of Burn-in suitability and delves into the realm of interconnection applications. It provides a detailed demonstration of the uPads' functionality for testing purposes [11]. The findings shed light on the practical aspects of utilizing uPads for interconnection applications, indicating their potential value in a broader range of testing scenarios.

These results hold significant promise for the electronics industry, as Burn-in testing is crucial for ensuring the reliability and longevity of electronic components. By showing that the uColumns on the SDI meet the stringent requirements for Burn-in applications, the study provides a basis for their integration into electronic devices, enhancing their overall performance and dependability.

Additionally, the study's exploration of uPads for interconnection applications opens new avenues for efficient and effective testing procedures. The successful demonstration of uPads' functionality in this context suggests the possibility of streamlining testing processes and improving the overall testing accuracy in various electronic manufacturing stages.

6. Acknowledgments

Intel Guadalajara Design Center's sponsorship made this study possible, providing essential support and resources. It

holds great significance for future projects and has led to valuable insights and advancements in the field. The researchers are deeply grateful for Intel's support, which made this study a reality and paves the way for future innovations in electronics and technology.

The researchers express their gratitude to Centro de Tecnología Avanzada for providing the motivation that drove this study. Centro de Tecnología Avanzada's unwavering support and encouragement served as a catalyst for collaboration and innovation among the researchers.

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