A 2× VOLTAGE GENERATOR ANALYTICAL MODEL

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ABSTRACT

Since portable systems and processing power applications demand efficient power consumption, this paper deals with the development of an analytical model based on the on-resistance effect of MOS switches to design a silicon-based char-pump voltage generator (VG). This model that is developed for adding design parameters under the designer's control is a useful design tool to quickly estimate the VG's performance in the time domain. Numerical results are compared with transistor-level simulation to validate not only the analytical model, but also to estimate the integration area of a silicon-based VG. It was found that an on-resistance ranging from zero to 50 Ω presents a relative error of 2%. Experimental results show the usefulness of the proposed design model.

KEYWORDS: *Keywords*: CAD; circuit theory; power electronics
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1. INTRODUCTION

POWER DISSIPATION is currently a limiting factor to increase the efficiency of voltage generators (VGs). A VG also called DC-DC converter is essential in personal portable devices (PPDs) to energize circuitry needed for satisfying customer requirements. Numerous VGs have been developed for various PPDs, from circuits based on charge-pump techniques, to circuits based on LC networks [1]-[3]. The latter, however, demand high integration area that makes the proposal an expensive solution. Char-pump circuits, on the other hand, require capacitors, MOS-based switches, and a clock generator, i.e. it uses CMOS compatible components. Even when VGs based on the char-pump technique demand lower integration area than other approaches, remains a problem: the output voltage presents a ripple that depends on both the switching frequency and the on-resistance of switches. In this paper, an analytical model for designing a VG based on the char-pump technique is presented. Since this proposal includes parameters under the designer's control, an estimation of integration area is easily estimated. Numerical results and transistor-level spice simulations are compared in order to estimate the range on which not only the parameters under the designer's control fit the spice response, but also to offer a suitable design model for designing a MOS-based VG. The proposed model focused to develop a 2× voltage generator is based on technological parameters of 1.5 μm CMOS process.

2. THEORETICAL BACKGROUND

In this section, we will formulate the analytical modeling and compare its results with transistor level simulation for validating the proposed model. The circuit under analysis is shown in Fig. 1.

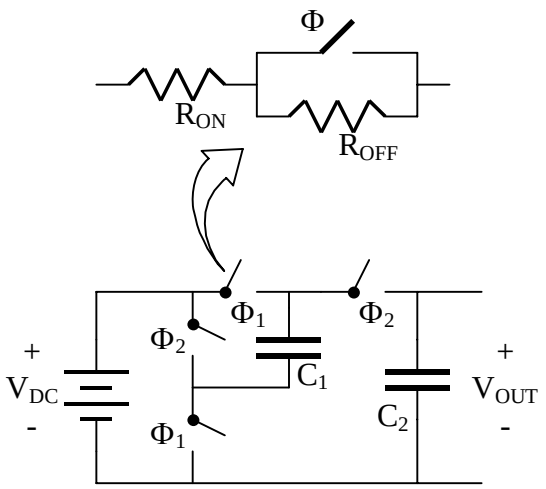


Figure 1. Circuit diagram and the model used for each switch.

Each ideal switch includes two lumped parameters: the *on*-resistor and the *off*-resistor. Assuming that the switch is a MOS transistor, R_{on} represents the non-zero resistance of the inversion channel, while R_{off} models the off state of the transistor. The latter is of the order of $10^9\ \Omega$ [4].

The circuit is operated by two-phase clock signals (Φ_1, Φ_2) that control the char-pump process between the capacitor C_1 and C_2; in this analysis C_1=C_2. In order to analyze the operation of the circuit, it was taken in account a pair of considerations: 1) the duty cycle of the clock is ½, and 2) a load (not shown in Fig. 1) is demanding a current I_{LOAD} to the circuit. When Φ_1=**1** (Φ_2=**0**) the voltage in the capacitor C_1 is V_{DC} while the voltage variation in the capacitor C_2, due to the current demanded by the load, is given by

$$\Delta v_{C2}(t,\Phi_1) = \frac{I'_{LOAD}}{C}\cdot\frac{T}{2} \qquad (1)$$

where T is the clock period and C=C_1=C_2. When Φ_2=**1** (Φ_1=**0**), the current demanded by the load is supplied by both capacitors causing an unwanted voltage variations. One of them, i_2, causes a variation in the voltage drop across C_2 given by [5]

$$v_{C2}(t,\Phi_2) = \frac{i_2}{C}\cdot\frac{T}{2} \qquad (2)$$

where i_2=½I'_{LOAD}. Then

$$v_{C2}(t,\Phi_2) = \frac{I'_{LOAD}}{C}\cdot\frac{T}{4} \qquad (3)$$

From (1) and (3) the total voltage variation in C_2 is easily obtained:

$$v_{C2}(t) = \frac{3}{4}\cdot\frac{I'_{LOAD}\,T}{C} \qquad (4)$$

For deducing (4) it was assumed that charge losses in C_2 at the phase Φ_1 is compensated by the charge that C_1 supplies to C_2 at the phase Φ_2. Consequently, V_{C1} suffers a variation given by

$$v_{C1}(t) = \frac{3}{4} \cdot \frac{I'_{LOAD}\, T}{C} \qquad (5)$$

However, since the capacitor C_2 is supplying all the time current to the load (see Fig. 2), a ripple with magnitude $½V_{C2}(t)$ appears on the output voltage. This voltage is given by

$$v_{OUT}(t) = 2V_{DC} - \frac{3}{4} \cdot \frac{I'_{LOAD}\, T}{C} - \frac{1}{2} \cdot \frac{3}{4} \cdot \frac{I'_{LOAD}\, T}{C} \qquad (6)$$

where the first terms is the ideal response, and the second term is the voltage variation due to the charge losses in C_1. Then

$$v_{OUT}(t) = 2V_{DC} - \frac{9}{8} \cdot \frac{I'_{LOAD}\, T}{C} \qquad (7)$$

Equation (7) indicates several design strategies to minimize not only switching effects, but also to diminish the ripple magnitude. The latter is given by

$$v_{RIPPLE}(t) = \frac{3}{4} \cdot \frac{I'_{LOAD}\, T}{C} \qquad (8)$$

Even when I_{LOAD} represents, for the context of this analysis, an incremental current variable, the current required by the load is enough once I'_{LOAD} reaches its final value, i.e. $I'_{LOAD}=I_{LOAD}$. Results given in (7) and (8) assume a zero on-resistance.

A. The on-resistance effect

In order to determine now the effect of the on-resistance on the output response, the lumped circuit shown in Fig 2. is analyzed.

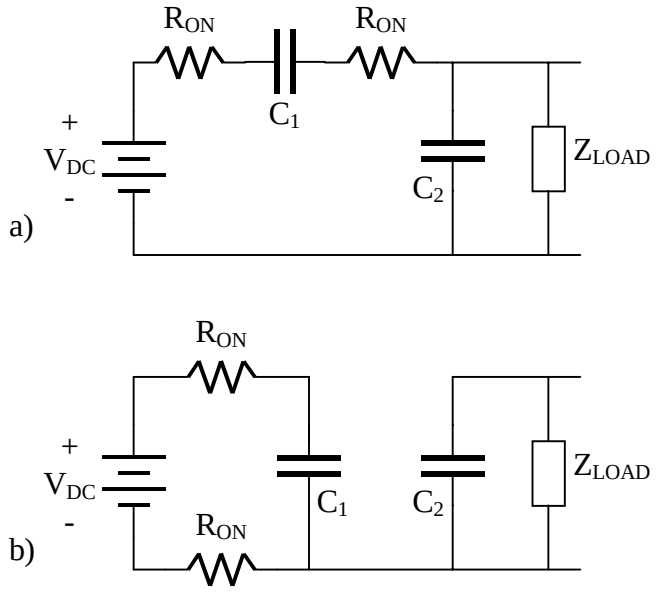


Figure 2. Equivalent circuit for time domain analysis. Φ_2=1 (a), and Φ_1 =1 (b).

This circuit is actually the resulting one for each clock phase. By using networks theory and Laplace transform, it was found that the output voltage is given by (9), where T_2 is the time in which C_2 supplies

charge to the load, and T_3 is the time in which C_2 receives charge from C_1 [6]. Fig. 3 depicts the voltage variation in C_2 versus time. At the phase Φ_1=**1** the figure illustrates how the voltage V_{C2} is falling down due to the current i_2 that C_2 supplies to the load. Next, at the phase Φ_2=**1** two time periods are identified: T_3 and T_2. While the first one defines the time that C_1 requires to supply current to the $Z_{LOAD}C_2$ network, T_2 starts when both capacitors reach the equilibrium. At the time T_2, C_2 is also supplying current to the load, and an unwanted voltage variation appears.

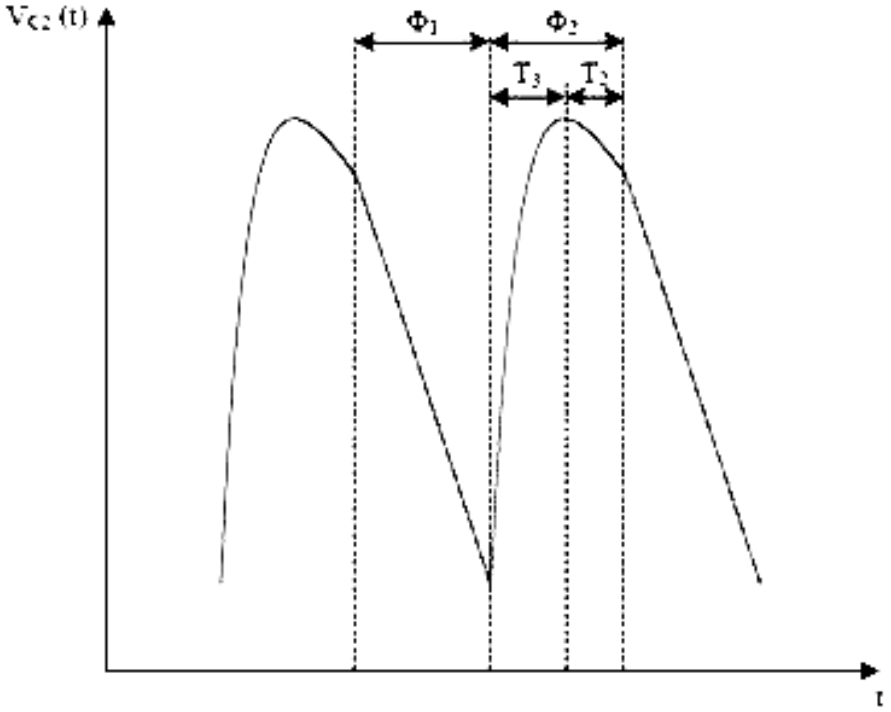


Figure 3. Voltage variation $V_{C2}(t)$ vs time.

3. THEORETICAL RESULTS

In this section a results comparison between analytical model and transistor level simulation is carried out with a discussion of required circuits to design a whole VG. Fig. 4 shows results calculated from (9) and spice simulations (circuit shown in Fig. 2) as function of R_{on}.

$$V_{OUT}(t) = 2V_{DC} - \frac{3}{4}\cdot\frac{I_{LOAD}T}{C}\left(1+\frac{8R_{ON}C}{3T}\right)\left(1+\frac{T_2}{T}\left[1-Exp\left(-\frac{T_2}{R_{ON}C}\right)\right]\right)-\frac{T_3}{C}I_{BIAS}\left(1+4\frac{R_{ON}C}{T}\right)-2I_{LOAD}R_{ON} \quad (9)$$

Spice simulation was performed by choosing an ideal switch including its on-off characteristics, a power supply V_{DD}=1.5 V, sampling frequency f_s=250 kHz and capacitors C=100nF. During simulations, the changes of voltage across the capacitor C_2 as a function of R_{on} were compared with the calculated values from (9). A high density of points is shown in Fig. 4, where a relative error between both approaches of 1.18% was found. This figure also shows the simulation result of a transistor-based char-pump circuit, where transistors were sizing in order to obtain an on-resistance of 20Ω (see Fig. 5). The latter was performed according technological design rules of a 5V, 1.5μm CMOS fabrication process.

Transistor based simulations include peripherals embedded in the char-pump circuit, including one voltage-controlled oscillator VCO, one boost circuit, one p-n diode, digital buffers, and one two-phase clock generator.

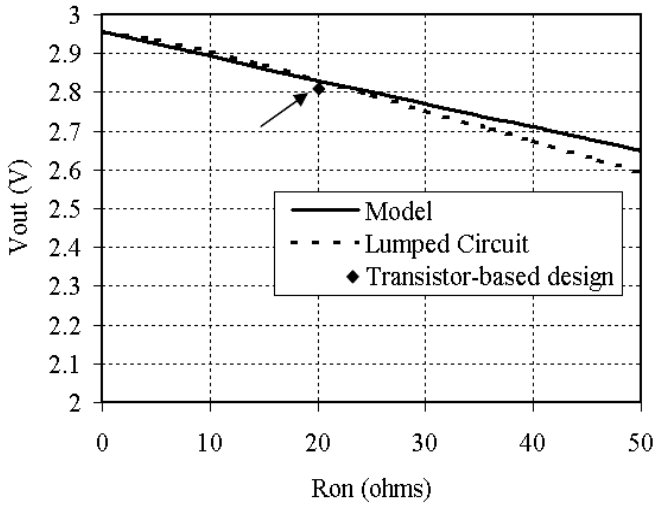
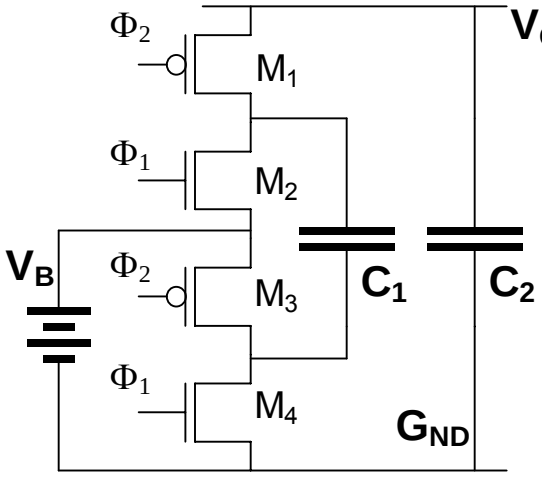


Figure 4. Voltage variation $V_{C2}(t)$ vs time. The maximum relative error between results was 1.88%.

Fig. 5 shows the MOS-based char-pump circuit. While the VCO has an amplitude equal to V_B, the boost circuit is powered via $V_{OUT}=2V_B$. However, since at the time t=0 the output voltage is ideally zero, the level shifter circuit is powered with the voltage given by the series connection of the source V_B and the p-n diode (not shown in the figure). Once the time runs the output voltage increases up to the p-n diode is turned-off. At that time the VG is already able to bias by itself to the boost circuit, two-phase clock generator, and digital buffers.



Transistor	W/L
M_1	2172/1.8
M_2	3380.4/1.8
M_3	5700.6/1.8
M_4	650.4/1.8

Figure 5. Sizing of transistors produce an equivalent on-resistance of 20Ω.

4. PRELIMINARY EXPERIMENTAL RESULTS

In this section, the voltage response of some basic blocks measured from a home-made automatic test environment (ATE) based on a PSoC is presented for a comprehensive analysis of the char-pump circuit's performance. The measurements are obtained with help of digital buffers connected to output

nodes. These buffers, embedded in the test chip, drive a load of 25pF. Fig. 6 shows the room temperature response of a 43-stage VCO versus time, where the voltage source V_{DD} emulates a battery V_B=1.5V. In order to obtain experimental data the ATE applies a constant voltage V_B to bias the VCO and also an incremental voltage V_C to the gate of a control transistor. Since this transistor (not shown in Fig. 6) controls the current driven by the NOT circuits, the frequency of the clock Φ is under the designer's control. As illustrated in Fig. 6, a voltage V_C=0.7 V is enough to generate a clock signal of 251.3 kHz.

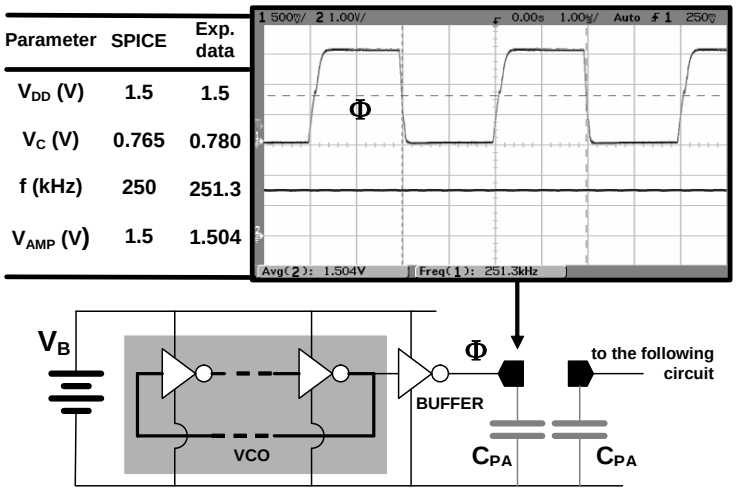


Figure 6. Simulation results fit in high percentage experimental values.

In practice, if the frequency response is measured as function of the control voltage at a constant bias voltage V_{DC}, the curve shown in Fig. 7 results. The response corresponds to the nine-stage VCO reported in [7]. This result shows that the VCO operate correctly at low bias voltages. A common figure-of-merit in digital design to save power is by applying a bias voltage lower than the sum of both basic threshold voltages, ($V_{Tn}+|V_{Tp}|$). In order to measure an acceptable frequency value a window of 1 second was defined to measure the output response. The window time is controlled with help of an external crystal, while frequency is measured with a resolution of 15.6 mHz. The frequency value is measured with help of the ATE. The frequency-voltage characteristic is downloaded to a PC via the RS-232 interface. Since the PSoC (CY8C29466, Cypress) is a mixed-signal device, several embedded modules in the PSoC were use to build an 8-b communication channel for a transmission rate of 9600 baud [8].

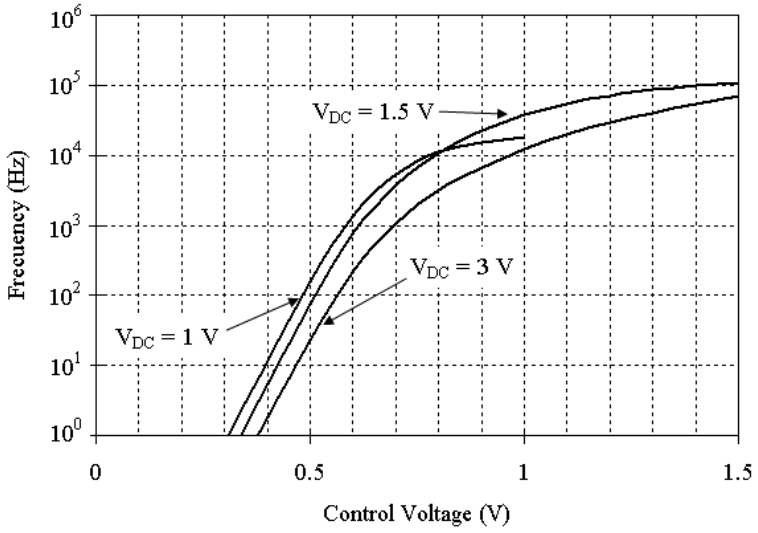


Figure 7. Experimental results obtained from a nine-stage VCO.

Fig. 8 shows a comparison between transistor-level spice simulation and experimental results. These results indicate that the proposed analytical model is a useful design tool to estimate quickly the response of a char-pump circuit by taking in account design parameters. Unfortunately, the magnitude of the ripple suffers from several non-ideal properties that must be characterized and compensated for (see Fig. 8). Based on preliminary results, a design strategy based on experimental data will be feed back to enhance the usefulness of the proposed model.

Parameter	SPICE	Exp.data
V_{OUT} (V)	2.82	2.72
V_{RIPPLE} (V)	0.022	0.028
Efficiency	91%	90%

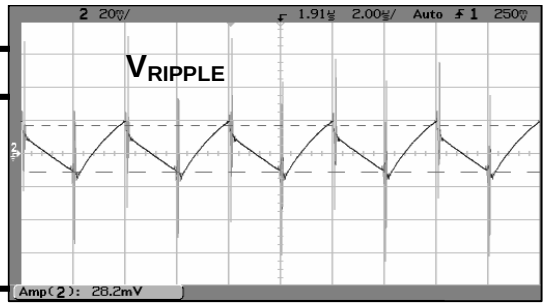


Figure 8. Experimental data present lower/higher output/ripple voltage that the theoretical results.

5. CONCLUSIONS

An analytical model based on the on-resistance effect of MOS switches to design a silicon-based char-pump voltage generator (VG) has been developed and discussed in detail. The model allows designers to add design parameters to estimate the output response and the effect of these parameters in the magnitude of an undesirable ripple. The model design leads to very simple equation that can be used in a pencil and paper design procedure. Then, from these results a MOS-based VG has been designed according technological design rules of a 1.5μm CMOS technology. Analytical results were compared with transistor-level simulation to validate the design model. The comparison shows that an on-resistance ranging from zero to 50 Ω presents a relative error of 2%.

In this paper, spice results and experimental data were also compared. The comparison shows that a VG based on switches with R_{on}=20Ω generates an output voltage lower than the spice response, which means a relative error of 1.18%. In contrast, the magnitude of the output ripple was higher that the

expected one. The latter represents a relative error of 27%. The development of a design strategy to minimize the amplitude of the ripple is mandatory.

6. REFERENCES

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