PERFORMANCE OF A MFS-BASED MOSFET FOR LOW TEMPERATURE APPLICATIONS

P.J. García-Ramírez[1] & F. Sandoval-Ibarra[2]

[1]Facultad de Ingeniería de la Universidad Veracruzana
Calzada Ruiz-Cortinez # 455, Boca del Río,Veracruz México
& Universidad Cristóbal Colón, Carretera La Boticaria s/n
Veracruz, Veracruz, México
jagarcia@uv.mx

[2]CINVESTAV,Guadalajara Unit, Prol. Av. López-Mateos Sur # 590
45235 Guadalajara, Jalisco, México
sandoval@cts-design.com

Received: November 7th, 2003. Accepted February 25th

ABSTRACT

A split-drain MAGFET has been designed for detecting magnetic fields at very low temperature. In this design a key parameter is the Hall angle, which indicates the current line deviation due to the Lorentz force acting on the charge carriers. It is well known that reducing the work temperature the carrier mobility increases, therefore an increase in carrier deflection is expected. As a consequence the split-drain MAGFET is able to detect magnetic fields below 1mT at 77K with low power consumption. Experimental results of a wide temperature range (20K<T≤300K) are presented.

RESUMEN

Un sensor MAGFET de separación de drenajes es diseñado para detectar campos magnéticos a muy bajas temperaturas. En este diseño el parámetro base es el ángulo-Hall, el cual proporciona una variación en corriente debida a la fuerza de Lorentz que actúa sobre los portadores en movimiento. Es bien sabido que reduciendo la temperatura de trabajo se incrementa la movilidad de portadores, por tal razón se espera un incremento en la variación en corriente. En consecuencia, el MAGFET es capaz de detectar campos magnéticos menores a 1mT a una temperatura de 77K con bajo consumo de potencia. Se presentan resultados experimentales en un rango de 77K a 300K

KEYWORDS: Sensors, Integrated circuits

1. INTRODUCTION

A common practice for detecting Magnetic Fields is to exploit galvanomagnetic effects due to the action of the Lorentz force on the charge carriers [1]. In semiconductor materials the carrier mobility, as well as the magnetic induction, causes the sensitivity to magnetic fields [2]. Thus, high charge carrier mobility is crucial for achieving high sensitivity and, most important, if circuit conditioning has to be integrated with the sensor device, the fabrication process has to be non-expensive and reproducible. Actually, silicon has not high mobility but it is cheaper and offers the unique advantage of magnetic field sensors (MFS) compatibility to CMOS technology [3]. Recently, the MFS have

experienced an exponential growth [4-6], but the theoretical understanding of the electronic mechanisms underlying these devices has not kept up with this growth. In order to analyze silicon devices in the presence of magnetic fields a semi-analytic model was developed in [7]. Using such model, we have obtained an optimum split-drain MAGFET design. It was incorporated in a trial chip that was fabricated and tested at a wide temperature range (20K<T≤300K). Since the corresponding electronics are used to process the signal delivered by the MFS, it is mandatory not only to integrate the circuitry as close as possible to the MFS but also to understand how to avoid undesirable cryogenic-effects in order to diminish the circuitry deterioration. Therefore, it is basic to generate a temperature-dependent SPICE model for the MOS transistor. The aim of this paper is mainly to describe the low-temperature performance evaluation of a MFS for detecting magnetic fields. To facilitate the exposition, basics for the split-drain MAGFET design are given in section 2, experimental results are described in section 3, and finally, in section 4, the conclusions of this work are given.

2 PHYSICS OF THE SPLIT-DRAIN MOSFET

Applying a magnetic field $\vec{B}$ to a charge carrier flow, which is moving through a quasi-straight path, causes a path change of the current flow towards a non-linear trajectory [8]. The deflection of electrons under $\vec{B}$ can be estimated by solving the equation

$$F_M = \frac{m_n^*}{|\vec{B}|}\left(\vec{r_c} \times \vec{B}\right), \qquad (1)$$

where $\mathbf{m^*_n}$ is the effective mass of electrons, and $\mathbf{r_c}$ is the cyclotron radius. As equation (1) shows, the higher the cyclotron radius is the higher is the magnetic force that translates to a larger carrier deflection. That is true when the region in which electrons flow is not only uniform (free of surface effects) but is also thinness. The magnetic field, whose direction is normal to the plane of the structure, causes a deflection of the lines of the current flow in the channel region.

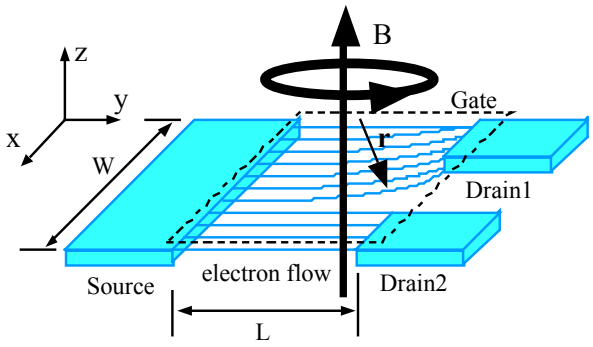

Figure 1. Deflection of electrons under the influence of a magnetic field. W and L are the width and length of the MOSFET inversion layer, respectively. The gate is not shown

With the split-drain structure (see Fig. 1), the MAGFET is able to sense the magnetic field which is perpendicular to the channel of the device. Since last century the MOS transistor inversion layer has been used as a suitable magnetic field sensor. From the MOS transistor theory, we can consider that the effective mass of electrons is related to the channel mobility μ_s, therefore the cyclotron radius is function of $1/\mu_s$. This fact is important because the current line deflection is strongly related to the charge carrier mobility. In other words, the higher the carrier mobility is the shorter the curvature radius. At room temperature silicon does not have high mobility, however the mobility increases as temperature is lowered; therefore one expects a larger deflection of the current lines at cryogenic temperatures.

The physical mechanisms that govern carrier mobility have been studied since the 50's, when Sonder and Stevens [9] obtained Hall coefficients by measuring magnetic susceptibility of n-type silicon with a wide range of donor concentrations as a function of temperature (3K ≤T≤ 400K). In 1994, Hochwitz and Henning used the Ridley Third Body Exclusion model and neutral impurity scattering to predict low field mobility over a wide range of temperature (70K ≤T≤ 300K) and doping concentration [10]. Another work presents the influence of the oxide-charge distribution on electron mobility in MOS transistor from 77K to room temperature. In that work, it was found out that the charges located at 100Å or more modify electron mobility [11]. In all these works the authors found out that the experimental results are in good agreement with their model predictions, however, for very low temperatures (T<20K), there are additional effects that they did not take into account to enhance their carrier mobility models. In practice, the design of a MFS must be separated in two basic areas. One of them is to find the Split-Drain MOSFET optimum size in order to enhance its sensitivity, while the last one is focused on the cryogenic effect on the MOS transistor performance. The latter is a mandatory analysis not only for circuitry integration but also to understand how to avoid undesirable cryogenic non-idealities in order to minimize the circuitry deterioration. In this work we have focused our attention on developing a CMOS compatible MFS.

2.1 Basics on MFS

Since the carriers deflection effects at low temperature are enhanced, we have designed a split-drain MAGFET. The Fig. 1 shows a magnetic induction vector perpendicular to the inversion layer, which produces a current imbalance $\Delta I_{DS}=(I_{D1}-I_{D2})$ between drains. In order to deduce the optimum size of the device, the magnetic sensitivity is defined in terms of the relative drain current difference per magnetic induction [12], this is

$$S_R = \left| \frac{\Delta I_{DS}}{I_{DS}\ \vec{B}} \right|, \tag{2}$$

where I_{DS} is the current supplied by the source region of the MOS transistor. The applied mathematical analysis to develop the split-drain MOSFET can be found in [7], where basically a semi-analytic model based on semiconductor physics and electromagnetic theory was developed. A short description of the proposed model is described by the following equations

$$m^* \frac{d^2x}{dt^2} = q\vec{B}_z \frac{dy}{dt}, \tag{3a}$$

$$m^* \frac{d^2y}{dt^2} = -q\vec{B}_z \frac{dx}{dt} + q\frac{V_{ds}}{L}, \tag{3b}$$

$$m^* \frac{d^2z}{dt^2} = \frac{q\sqrt{2}kT}{qL_D}\left\{ e^{-\frac{\psi_s}{V_t}} + \frac{\psi_s}{V_t} - 1 + \frac{n_{po}}{N_b}\left[e^{\frac{\psi_s}{V_t}} - \frac{\psi_s}{V_t} - 1 \right] \right\}, \tag{3c}$$

with

- ψ_s surface potential
- V_t thermal voltage
- k Boltzmann constant
- L_D Debye length
- N_b bulk doping concentration
- n_{po} concentration of electrons in thermal equilibrium in p-type semiconductor
- T absolute temperature.

The carrier's trajectories are obtained by solving (3) using the inverse Laplace transform method with suitable initial conditions. Once the carrier's deviation was obtained, the following task is to evaluate the time that electrons spend along the channel. Next, it is possible to find the carrier deflection under the influence of a magnetic field along the width **W** of the MOSFET. In this analysis we assumed that the split-drain MAGFET has large size, therefore, the mismatch can be neglected.

2.2 DESIGN OF THE SPLIT-DRAIN MAGFET

Considering a constant and uniform magnetic field as well as technological parameters, it is simple to obtain the magnetic sensibility as function of the transistor size. Fig. 2 shows the influence of the channel length on the sensibility (%/T). It was found that the maximum sensitivity of the MFS is approximately given by **L**=4**W**. As L becomes larger the magnetic sensitivity reduces its value because of the distance between source and drains. That means that the cyclotron radius causes a carrier's path deviation such that the carrier does not reaches the drain and the current imbalance tends to zero. In such a case, for detecting magnetic fields Hall voltage measurements must be done. On the other hand, let us suppose **L** has minimum size. The distance between source and drains is so short that carriers do not suffer a detectable path deviation and the current imbalance is almost zero because that the current in each drain presents practically equal magnitude. According to the results shown in Fig. 2, the proposed split-drain MAGFET size is (W/L)=(100μm/400μm) with an **n**-type polysilicon gate electrode.

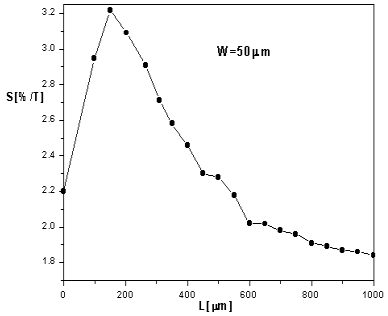

Figure 2. Calculated magnetic sensibility versus channel lengths L. In this analysis $B=50mT$, $V_{DS}<V_{Dsat}$.

3. EXPERIMENTAL RESULTS

The fabrication of the split-drain MAGFET begins using **p**-type, <100> 3-in silicon wafers. All technological steps were performed with the use of IC technological line and photolithography masks with a minimum line definition of 5μm at the Microelectronics Laboratory, Puebla (México). The set-up shown in Fig. 3 permits making current imbalance over the temperature range 20-300K. A dc current (from 0 to 1400mA) through the electromagnet is controlled using a variable resistor in order to produce a magnetic field **B** in the 0-80mT range. The device-under-test (DUT) was applied in the electromagnet in such a way that **B** is considering uniform. Data were taken using the HP4156A Semiconductor Parameter Analyzer, which has a personal-computer interface for visualization purposes.

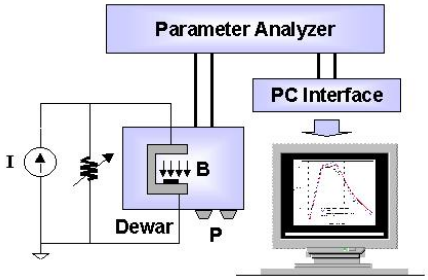

Figure 3. Diagram of the set-up used for current imbalance measurements. The label P indicates the points where a vacuum pump is connected.

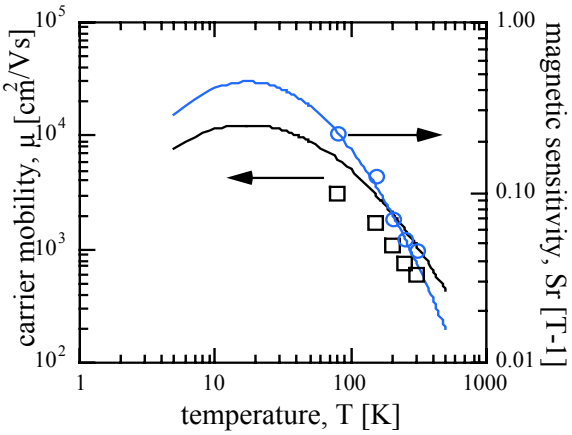

Figure 4. Measured (symbols) and calculated (lines) carrier mobility μ (squares) and magnetic sensitivity S_I (circles) versus temperature (4.7K to 300K)

The mobility μ and magnetic sensitivity S_I were estimated from the model and compared to extracted data (see Fig. 4). The increment in the deflection of the current lines is confirmed by the augment in both carrier mobility and magnetic sensitivity in the whole temperature range; however, the experimental data were gathered only from 77K to room temperature, where mobility is mainly dependent of lattice vibrations. Therefore, the lower is the temperature the lower is the phonons density. The differential current measurement at 77K is shown in Fig. 5, where not only a magnetic field of 50mT was applied but also stable biasing were supplied (V_{BS}=0, V_{DS}=1V).

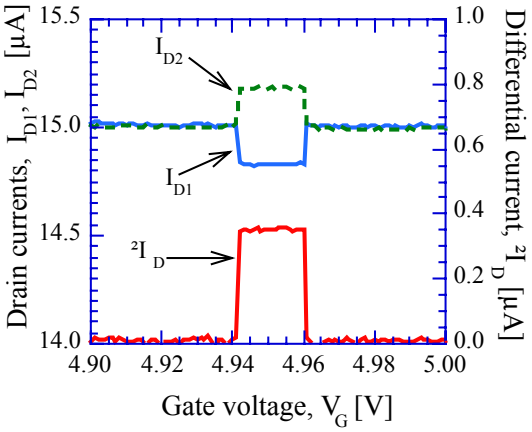

Figure 5. Experimental drain currents I_{D1}, I_{D2}, and differential current ΔI_D of a MAGFET operated at 77K

As we have seen, one of the drain regions drains the current that the other one losses. Thus, the magnitude of the differential current, ΔI_D, is $0.35\mu A$, which represents a magnetic sensitivity of the order of $0.23\ T^{-1}$. Fig. 6 shows the temperature dependence of the NMOS threshold voltage V_{Th}. Each datum was extracted from the linear region of the drain-current/gate-voltage characteristics, in which a bias V_{DS}<50mV was used. As a first approximation the temperature dependence of the threshold voltage can be predicted by

$$V_{Th} = \begin{cases} V_{T_0}\left(\dfrac{301-T}{21.28}\right)^{0.14095}, & 10K \le T < 250K \\ V_{T_0}(301-T)^{0.0308}, & 250K \le T < 300K \end{cases}, \quad (4)$$

where V_{To} is the threshold voltage at room temperature. It is clear that from 120K down to above 20K, the V_{Th} has a different performance as predicted by (4). The utility of this parameter is important because there is a strong interest to develop a suitable SPICE model for the MOS transistor in order to design the required circuitry for signal processing. It is well known that integrating in the same chip sensors and circuits several non-desirable effects are avoided. The development of a SPICE model will be described in a future paper.

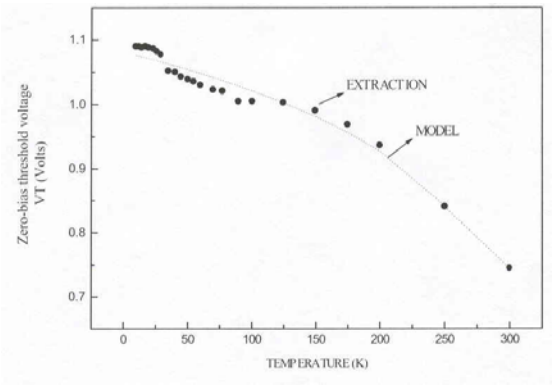

Figure 6. The experimental extracted data (V_T) as a function of temperature

4. CONCLUSIONS

The development of a split-drain MOSFET for magnetic field detection at 77K has been designed and tested. The results are in good agreement with the model prediction. The power consumption is of about $150\mu W$ at $77K$ with a S_r=0.23 T^{-1}, while at room temperature the consumption is $110\mu W$ with a S_r of 0.045 T^{-1}. As we can see, the magnetic sensitivity increases 5.1 times its value when cooled from room temperature down to 77 K. This implies that the minimum magnetic field B_{min} to be sensed could be reduced down to the range of μT.

5. ACKNOWLEDGMENTS.

The authors would like to thank the experimental assistance of M. Landa and M.Sc. C. Zuñiga at the Microelectronics Laboratory, INAOE, Tonantzintla (México).

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Authors biography

Federico Sandoval-Ibarra

Was born in San Luis Potosí, México. He received the B.E. degree in Physics-Electronics from the UASLP in 1988, México, and the Sc.D. degree in electronics from INAOE, México, in 1997. During 1991-1996, he was at Microelectronics Laboratory at INAOE as an assistance researcher developing wet-etching techniques as well as CMOS circuitry for silicon-based microsensors. In 1997, he was at CNM as a visiting researcher being involved in developing the surface micromachining techniques for a hearing-aid device. In 1999, he joined CINVESTAV, Guadalajara Unit, México, where he is currently the Coordinator of the Electronics Design Group. He is also an instructor, teaching CMOS mixed-mode IC design postgraduate courses. His design area includes silicon-based sensors, battery power management systems, $\Sigma\Delta$ modulators and class-E amplifier.