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EDITORIAL

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In this issue of *Computación and Sistemas* five articles and a Ph. D. thesis are presented. These works are described as follows:

In the first article Aguilar and Leiss investigate the increased response time problem on the Internet. Based on a proxy caching, they propose an adaptive cache coherence-replacement scheme. Their method, that takes into account both coherence and replacement decisions, permits the reduction of the costs for a proxy cache.

The second paper is focused on the feature selection based on typical testors. In this paper, Santos, Carrasco and Martínez propose a modification of this technique in order to be applied on a prediction problem handling astronomical data. The performance of their method is compared to other approaches. In particular, their show that the modified feature selection reduces about 50% the number of features.

In the next paper, Luna makes a study of the specification and analysis of real-time systems in type theory. In particular the author investigates a methodology combining the use of the model checker *Kronos* and the assistant *Coq* for the analysis of real-time systems and emphasizes the analysis of the railroad crossing example.

Fernández and Olmedo study the normative approach for decision-making, using methods of fuzzy preference relations in designing intelligent decision agents. Based on a multiobjective optimization and an evolutionary algorithm, the authors propose a novel method to achieve better solutions for the final prescription which is the main limitation of fuzzy preference methods.

In the final paper, Guevara, Medel and Cruz propose a dynamical model for a real-time task. Their model for arrival times and execution times, both based on ARMA models, permits the prediction of the behavior of the real-time task in a probability sense.

Finally, de Alba presents an abstract of his doctoral dissertation. His doctoral dissertation is focused on the study of loop instructions in order to increase the parallelism in the presence of loops. The author proposes a loop cache that includes hardware with a cache memory. The proposed loop cache allows to improve instruction level parallelism.

We would like to take this opportunity to thank all the authors for contributing their latest research results to this issue of *Computación and Sistemas*.

Dr. Iván Terol Villalobos
Associate Editor