1. Introduction

Magnetic field sensors (MFSs) have been common transducers in a lot of applications since decades ago. One of them is the industrial field, where dependence on the industrial activity work conditions could be critical. These work conditions refer to noise sources, uncontrolled temperature areas, humidity environments, and so on. Manufacturing industries, for example, control their processes by measuring/monitoring physical variables. Thus, these industries control their sensing procedures to satisfy mainly quality control indices [1]. Physical variables, on one hand, are then transformed into electrical values by using suitable transducers that, on the other hand, must fulfill conditions of high linearity, good SNR, and low sensitivity to environmental effects, among other requirements; otherwise, compensation circuitry is required mainly to minimize undesirable responses. That circuitry, however, introduces unwanted effects that may be reduced by integrating both transducers and circuitry within a semiconductor chip. Integrated sensors -systems made up of a fully-integrated transducer and circuitry- have been fabricated for several years using silicon-based technologies [2]. Nowadays, with the huge number of transistors in a chip, integrated sensors execute well-controlled functions at a moderate cost.

The MFS presented in this paper is an MOS-based split-drain MAGFET which can be used to sense magnetic fields (>100mT). A description of the setup is given as well as an electrical/magnetic characterization of the MAGFET, its relative sensitivity, and the equivalent circuit for transistor-level simulation purposes.

2. Background

In this section, the MAGFET operation is presented for a comprehensive analysis of magnetic field detection. In general, the magnetic sensing involves two steps:

1) the generation of the transistor channel for using it as an equivalent Hall plate, and

2) the measurement of a current imbalance between drains.

Let \( I_D \) be the transistor current operating under saturation conditions. In the following discussion, the case of a true response \( I_D=I_{D,IDEAL}+\delta I \), with \( \delta I \) the current contribution, due to undesirable effects, is considered. In order to eliminate the \( \delta I \) contribution the MAGFET is commonly integrated with compensation circuitry, and then the expected response is obtained. It must be noted that circuitry increases power consumption; however, since saving power is the design criterion of the success of integrated sensors, power consumption is minimized by integrating low-power differential circuits. The simplest differential circuit is the differential pair; this circuit has been recently designed to drive a current \( I_{BIAS}=1\mu A \) at \( V_{DD}=5V \), with \( 5\mu W \) static power consumption [3]. The differential technique takes advantage of the split-drain MAGFET structure, because for this particular design, the MAGFET response is due to the current imbalance between drains.

However, since the current driven by each drain is \( (I_{D,IDEAL}+\delta I)/2 \), at \( B=0 \), and also as a result of the charge carriers deflection due to \( B \neq 0 \), the current imbalance \( i \) can be obtained from current measurements:

\[
\Delta I = \left[ \frac{1}{2} (I_{D,IDEAL1} + \delta I) + i \right] - \left[ \frac{1}{2} (I_{D,IDEAL2} + \delta I) - i \right] = 2i
\]

\( i.e. \) the measurement of the differential current \( \Delta I \) is a measure of the magnetic field strength, \( I_B \). Because of the...
common-mode nature of unwanted effects, $\delta I$ is eliminated. Nevertheless, an unwanted current contribution can be generated with a low active area [4]. In this work, to measure a current $\Delta I \approx 0$, the active area of the transistor is $180 \times 90 \mu m^2$.

3. Measurements of $I_D$-V curves

In this section, the room temperature current-voltage characteristic measured from a home-made automatic test environment (ATE) is presented for a comprehensive analysis of the $\Delta I=0$ requirement [5]. The measurements are obtained with both drains connected to a common node. Figure 1 shows the room temperature $I_D$-V characteristic of the p-type MAGFET for three different gate-to-source voltages ($V_{GS}$) versus drain-to-source voltage ($V_{DS}$).

In order to obtain experimental data, the PSoC-based ATE applies a voltage to the gate of the transistor, and an incremental voltage at the source is also applied. The common drain includes an external resistor to measure the drain current via voltage measurements. The resistor voltage drop is also measured with the help of the ATE. The $I_D$-V curves, which are downloaded to a PC via an RS-232 interface, are needed to select the correct $V_{GS}$ voltage, because for this application, the relative magnetic sensitivity ($S_\Gamma$) of the MAGFET is a function of $1/I_D$.

Figure 2 shows the $\Delta I$ curve for three different $V_{GS}$ voltages with each drain connected to an external resistor. These curves were obtained at $B=0$. Notice how the three curves change over the $V_{DS}$ axes. The curve due to the voltage $V_{GS}=-5V$ rises from -120nA and reaches its peak (225nA) at a voltage $V_{DS}=-3.5V$. The curve for $V_{GS}=-3V$, on the other hand, presents the lowest error ($\approx 0.27\%$) over the $V_{DS}$ axes. The error, which is measured with the origin at $\Delta I=0$, does not reach the $\Delta I=0$ requirement except the voltage $V_{DS}=-2.75V$.

The curve for $V_{GS}=-5V$ presents the highest drain current (see Fig. 1), and diminishes to $\Delta I=0$ (see Fig. 2) at about $V_{DS}=-(3.875\pm0.125)V$. Under these operation conditions the MAGFET is then tested by applying a magnetic field perpendicular to the chip surface ($\approx 2.0 \times 2.0\,mm^2$). The test chip is packaged in a LCC28 unit.

4. Test methodology

In this section, the test procedure is presented with a discussion of the current imbalance measurement to calculate the sensitivity of the MAGFET. In general, the test sequence involves two test aspects:

1) the development of a mechanical platform based on a pair of magnets, and

2) the use of a commercial MFS to quantify the magnetic field strength of the parallel magnet array.

Figure 3 shows the mechanical test platform. Magnets, with a size of 10 cm diameter and a gap $h_3=1.2\,cm$, form a parallel system. The upper magnet presents an up/down movement, whereas the bottom one is fixed to the base. The active area to test the chip, or DUT, is an area located around the geometrical center of the bottom magnet’s upper face. That area defines the region where magnetic field lines are perpendicular to the chip’s surface. Furthermore, since the magnitude of $I_B$ is inversely proportional to the distance $r$, the movement of the upper magnet satisfies $r \geq h_3$. The gap, on the other hand, defines the minimum distance for handling the test chip.

4.1. Measurement of the $I_B$-$r$ characteristic

A commercial MFS was used to quantify the magnetic field strength of the parallel magnet array as a function of $r$ [6]. By assuming the data given by the manufacturer, the relative sensitivity of the MFS is calculated from the following model:

\[
S_B = \frac{1}{I_B} \left[ V_0 - V_0(I_B) \right],
\]

Figure 1. Static $I_D$-V curves of the split-drain MAGFET.

\[ \text{Figure 2. Static current } \Delta I \text{ as function of } V_{DS}. \]

\[ \text{Figure 3. Mechanical test platform.} \]
the high density of the points was used. Thus, the magnetic field strength $I_B$ (see Fig. 4) as a function of distance was found to be

$$I_B(r) = I_{B0} - 0.0628r,$$

where $|I_{B0}|=T$ and $I_{B0}=153.2\text{mT}$ corresponds to $I_B(0)=I_B(h_3)$. The observed response is a linear function of the distance over a $55\text{mT}$ range.

### 4.2. The MAGFET sensitivity

This transducer presents an aspect ratio $W/L=2$ with $W=180\mu\text{m}$. Figure 5 shows current measurements of both drains as a function of $I_B$ for several values of the gate voltage $V_{GS}$. The relative sensitivity of the MAGFET is obtained with the data from Fig. 5 according to the following model:

$$S_r = \frac{1}{I_B} \cdot \frac{i_{ID}}{I_D} = \frac{\alpha}{I_B} \cdot \frac{L}{W},$$

where $\alpha=1078 \times 10^{-3} \text{m}^2\text{V}^{-1}\text{s}^{-1}$ [7].

The voltage pulse technique requires that measurements be made on a short time scale, and that there be a higher relaxation time between measurements in order to avoid the Lorentz force effect. This effect causes charge carriers to modify their trajectory to a linear path, making the measurement of the current imbalance unpractical. From experimental results, the relative sensitivity of the MAGFET at room temperature was found to be $S_r=540\mu\text{T}^{-1}$.

### 4.3. Equivalent circuit

In order to develop an equivalent circuit, it was assumed that the total drain current $I_D$ of the MAGFET can be modeled as a pair of transistors with a common gate and source; each equivalent transistor would drive a current $0.5I_D$. Figure 6 shows the MAGFET with two adjacent drains and the lumped model proposed for electrical simulation purposes. Each cur-

$$\text{FIGURE 3. Schematic view of the mechanical test platform.}$$

$$\text{FIGURE 4.} \ I_B-r \ \text{characteristic at room temperature.}$$

$$\text{FIGURE 5. Current driven by each drain as function of } I_B.$$

where $S_B=25VT^{-1}$, and $V_O$ and $V_O(I_B)$ represent the output voltage for $I_B=0$ and $I_B > 0$, respectively. In order to reduce fluctuations of the measurement data, the average of

$$\text{FIGURE 6. Split-drain MAGFET and the lumped model proposal.}$$

Here $I_{BIAS}$ is equivalent to the total drain current.
rent source must be visualized as a Magnetic field Controlled Current Source or MCCS. From the point of view of simulation, the equivalent circuit allows the designer to take into account the sensor response in design suitable conditioning circuitry, where a low power single-ended differential pair is one of them.

5. Conclusions

In this paper, we presented the split-drain MAGFET operation for a comprehensive analysis of magnetic field detection. The MAGFET, fabricated using a 1.5µm CMOS technology, was first measured at transistor level to obtain the \( I_D-V_{DS} \) characteristic. The electrical characterization was done with the help of a home-made ATE, mainly to minimize human errors but also to have control of applied voltages. Observation of the \( I_D-V_{DS} \) characteristic for several voltage-to-source voltages revealed specific values of \( V_{DS} \) where the measurement of the differential current satisfies \( \Delta I=0 \).

The development of a mechanical platform to quantify the magnetic field strength as a function of distance was described with regard to obtaining the sensitivity of the MAGFET. However, since this transducer suffers from the Lorentz force effect, the test procedure used a voltage pulse technique. Since this technique requires that measurements be made on a short time scale \( \Delta t \), the ATE resources were used to satisfy this requirement.

From experimental results, a relative magnetic sensitivity \( S_r=540\mu T^{-1} \) was obtained. This MAGFET parameter was used to propose a lumped model based on common network components, which is suitable for electrical simulation purposes. Finally, based on the preliminary results presented in this paper, we conclude that a fully integrated sensor may be developed, using the same technology, if each external resistor is substituted by the integration of low-voltage active resistors, where the simplest one would be a diode-connected MOS transistor.

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1. V. Falconi-campos, Controla da Qualidade Total, Universidade Federal de Minas Gerais, 1992.