

EFFICIENT CIRCUIT IMPLEMENTATION OF MORLET WAVELETS

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Received: June 19th 2004 and Accepted March 3^d 2005

ABSTRACT

A family of versatile building blocks intended for the implementation of Morlet wavelets is proposed. The circuits are compact, fully programmable, and well suited for low-voltage and low-power applications. The resulting wavelet is temperature compensated and low sensitive to process parameter variations. Using current sources can independently control the main wavelet parameters. Hspice and breadboard results demonstrate the feasibility of both the wavelet realization and proposed circuits.

RESUMEN

Se presentan varios circuitos para la realización de ondas tipo Morlet "Morlet wavelets". Los bloques básicos son compactos, programables, y pueden ser utilizados en aplicaciones donde se requiera bajo voltaje de alimentación y bajo consumo de potencia. La arquitectura propuesta está compensada en temperatura y es poco sensible a la variación de los parámetros del proceso de fabricación. Las principales características de los circuitos son controladas por medio de fuentes de corriente. Resultados de simulación y experimentales de la onda y los bloques básicos, muestran la funcionalidad y versatilidad de los circuitos propuestos.

KEYWORDS: Wavelet Circuit Implementation, Translinear Circuits, Non-linear circuits, Analog Integrated Circuits.

1. INTRODUCTION

Programmable gaussian functions are often used in wavelet transforms for the time-frequency representation of signals. The wavelet transform is also used in image processors, data compression systems, analysis of biomedical signals, and complex signal analyzers [1-4]. The circuit implementation for this transform involves several repetitive building blocks with similar functional characteristics. Both linear and non-linear circuits are main functional blocks. Therefore, the implementation of wavelet transforms requires precise, compact, and fully-programmable circuit elements.

Recently, wavelet transforms have been implemented using digital circuit techniques [5-10]; however, the practical impact of these realizations in battery-operated systems has been limited mainly because they require large amounts of silicon area. Also, the implementation of the Continuous Wavelet Transform (CWT) has been reported in the literature [11-13]. A family of gaussian functions with identical window shape can implement the CWT. These windowing functions, known as "mother" wavelets, control the localization in time (or space) and frequency [1, 2]. Gaussian windows minimize Heisenberg's uncertainty principle for the time-frequency representation of signals. Also, gaussian functions are often used in adaptive algorithms, pattern classification, and radial basis neural algorithms [14-

17]. More recently, wavelet transforms have also been used in real time applications; e.g. hearing aid devices to improve the intelligibility in the presence of noise [18] and detection of transients in power systems [19]. The last systems are software based; hence the speed of such systems is rather limited by the data acquisition board (analog-digital and digital-analog conversions) and extensive computations. Analog solutions get ride of these drawbacks.

Gaussian circuit realizations have been recently reported in the literature [20-22]; however, in order to take full advantage of the computational properties of wavelet transforms, efficient and versatile implementations of gaussian function generators are required. In this paper, we propose several building blocks for the analog circuit implementation of fully programmable Morlet wavelets that fulfill these requirements. By using bipolar current sources, the peak gain, standard deviation and mean value can be independently programmed. In addition, the resulting structure is insensitive to both temperature and process variations. Although we focus on the implementation of the Morlet wavelet, which is generated by gaussian windows, the circuits may also be used for other applications.

Design considerations for the Morlet wavelet are discussed in section 2, followed by the building blocks description given in section 3. Simulated and experimental results showing the performances of the proposed structure are given in section 4, and finally the conclusions are given in section 5.

2. DESIGN CONSIDERATIONS FOR THE MORLET WAVELET

The mother Morlet wavelet is a modulated function composed of two quadrature components, characterized by the following equation:

$$w_{s,\tau}(t) = \left[\cos \omega_0 \left(\frac{t-\tau}{s} \right) + j \sin \omega_0 \left(\frac{t-\tau}{s} \right) \right] h_{s,\tau}(t), \quad (1)$$

where

$$h_{s,\tau}(t) = \frac{1}{\sqrt{s}} e^{-\frac{1}{2} \left(\frac{t-\tau}{s} \right)^2}, \quad (2)$$

and s and τ represent the scale and translation of the windowed function $h_{s,\tau}(t)$, respectively. The term $1/s^{1/2}$ in (2) is given for energy normalization at different scales [1-3]. According to these expressions, the circuit realization of Morlet wavelets requires normalized gaussian windows and two components in quadrature. A block diagram representation of these equations is depicted in Fig. 1.

Due to its complexity, the most critical building block is the normalized gaussian function circuit in which the peak gain must be adapted according to the scale parameter as shown in (2). In this work, the circuit implementation of both a gaussian function generator $h_{s,\tau}(t)$ and the imaginary component of the Morlet wavelet are presented.

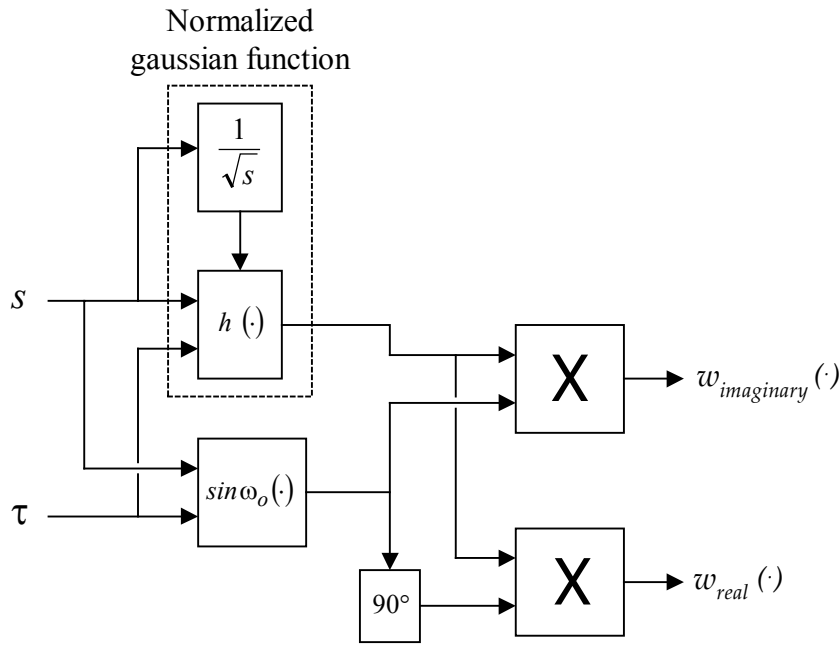


Figure 1. Block Diagram for the Morlet wavelet implementation

3. GAUSSIAN FUNCTION CIRCUIT IMPLEMENTATION

The proposed circuit realization is based on the translinear principle using bipolar devices [23]. The gaussian function circuit is composed of four basic building blocks: a two-quadrant squarer circuit, a linearized OTA, a gaussian function circuit, and a square root circuit. It can be noted in (2) that the exponent is always negative; hence four quadrant multipliers are not needed for its implementation, instead the two quadrant squarer shown in Fig. 2 is used [23].

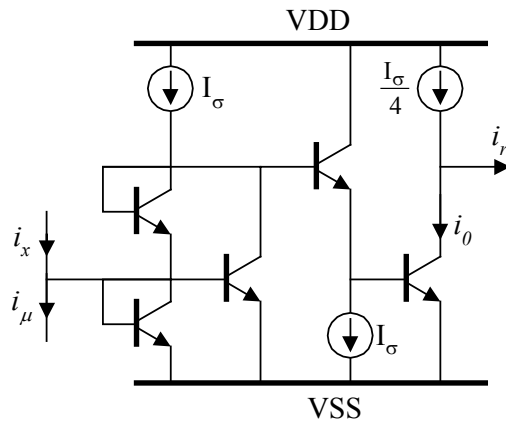


Figure 2. Two quadrant squarer circuit based on the translinear principle [23]

Neglecting the base currents and using typical circuit analysis techniques, it can be shown that the output current is given by the following expression

$$i_r = \frac{(i_x - i_\mu)^2}{4I_\sigma}, \quad (3)$$

where the currents i_r , i_x , i_μ and I_σ are defined in Fig. 2. It should be noted that for proper operation of the circuit the condition $(i_x + I_\sigma) > i_\mu$ must be satisfied.

If i_r is converted to voltage in a linear fashion by using a linear resistor, and the resulting voltage is converted to current by another bipolar transistor, the gaussian function is obtained. The basic principle is depicted in Fig. 3a [24].

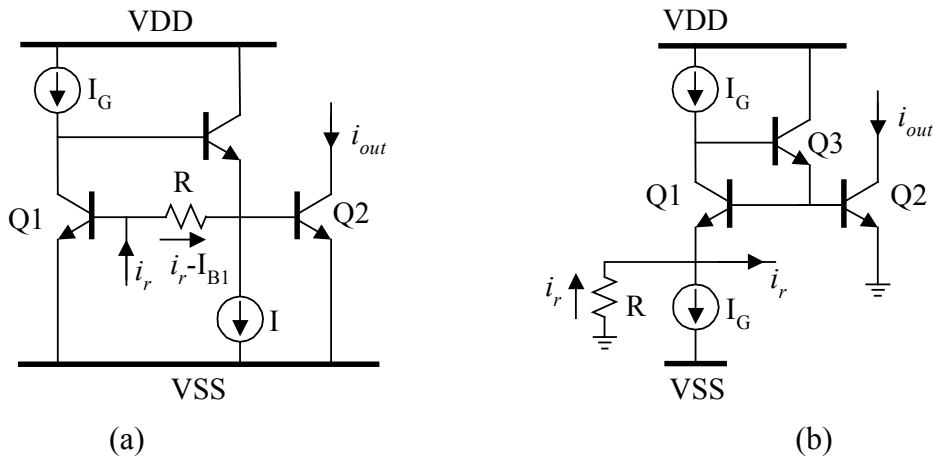


Figure 3. Current-mode gaussian function circuit using a) floating resistor [24] and b) proposed implementation using a grounded resistor

The input impedance of Q1 must be large enough to convert the output current of the two quadrant squarer i_r , given by (3), into the resistance voltage drop $v_R = Ri_r$. Hence, the internal voltage V_{BE2} is determined by the following expression

$$V_{BE2} = V_{BE1} - R(i_r - I_{B1}) = V_{BE1} - R\left(i_r - \frac{I_G}{\beta}\right), \quad (4)$$

where V_{BE1} is given by

$$V_{BE1} = V_{th} \ln\left(\frac{I_G}{I_S}\right). \quad (5)$$

Notice that in expression 4, we are not neglecting the base current I_{B1} ($=I_G/\beta$; β is the transistor ac current gain) because i_r might be very small. Q2 converts the equivalent voltage V_{BE2} to the output current. Using (4) and (5), the output current can be obtained as

$$i_{out} = I_S e^{\frac{V_{BE2}}{V_{th}}} = \left(I_G e^{\left(\frac{RI_G}{\beta V_{th}}\right)} \right) e^{-\left(\frac{Ri_r}{V_{th}}\right)}. \quad (6)$$

Notice in this equation that large resistors should be avoided otherwise the dc current flowing through the resistor might increase drastically the output current. If $RI_G \ll \beta V_{th}$, in accordance with (3) and (6), the output current for the gaussian function circuit can be expressed as

$$i_{out} = I_G e^{-\left(\frac{R}{V_{th}}\right) \left(\frac{i_x - i_{\mu}}{4I_G}\right)^2} \quad (7)$$

As can be seen in this expression, the output current represents the required gaussian behavior.

A proposed circuit implementation using a grounded resistor is shown in Fig. 3b. In this topology, due to intrinsic feedback (Q3), the impedance seen from the emitter of Q1 is relatively large ($\cong \beta_3 r_{\pi 2}$). The input current i flows through the resistor R , generating a small signal voltage drop proportional to the input current. This voltage is superimposed with the fixed base-emitter voltage of Q1, and it is converted into current by Q2. By using conventional circuit analysis techniques it can be shown that the resulting output current i_{out} is given by (7).

A drawback of the implementations shown in Fig. 3 is their temperature dependence ($V_{th} = kT/q$), as noted in equation (7). Besides, the output current depends on the absolute value of the resistance; typically it is temperature sensitive and its value is not well controlled in IC implementations. On-chip resistors present tolerances of around $\pm 30\%$. Fortunately, a resistor based on the small signal transconductance of a bipolar transistor compensates for these effects. For a bipolar transistor, its equivalent small signal resistance ($1/g_m$) is proportional to V_{th} , which cancels out the exponent of (7); hence, temperature invariance is achieved. Although a single transistor in diode configuration satisfies these conditions, its linear range is limited to less than ± 10 mV for low distortion applications. In this work the linearized operational transconductance amplifier shown in Fig. 4 is employed.

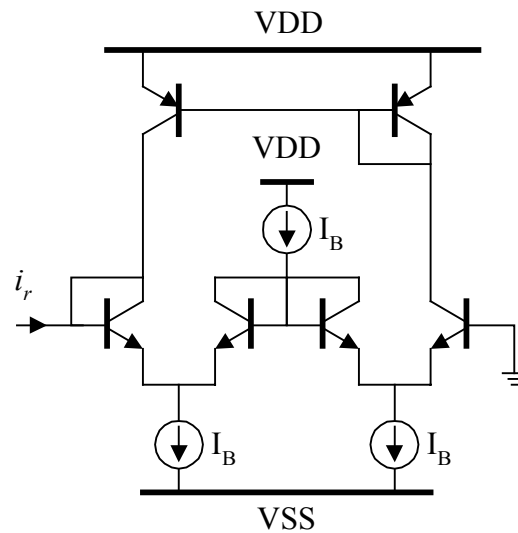


Figure 4. Linearized operational transconductance amplifier used as an active resistor to compensate temperature variations of the gaussian circuit

The amplifier connected in a unity gain configuration presents a small signal resistance given by

$$R = \frac{4V_{th}}{I_B} \quad (8)$$

Note that the condition $R \ll \beta r_\pi$ (required in equation 7) can be easily guaranteed. Using expression (8) into (7), the output current for the gaussian function circuit becomes temperature insensitive, and the input/output relationship yields

$$i_{out} = I_G e^{-\frac{(i_x - i_\mu)^2}{I_B I_\sigma}} \quad (9)$$

The resulting structure is accurate and versatile. According to this result, by using the currents I_σ , i_μ and I_G the gaussian output current parameters can be independently programmed. The current source I_σ is used to control the scale of the gaussian window while the translation is adjusted by the current source i_μ . The peak current gain is programmed by the current source I_G , and the current source I_B can be made proportional to the scale control current ($I_B = I_\sigma / 4$), and the output current becomes

$$i_{out} = I_G e^{-\frac{4(i_x - i_\mu)^2}{I_\sigma^2}} \quad (10)$$

leading to a compact, precise and versatile gaussian function circuit.

4. MORLET WAVELET CIRCUIT IMPLEMENTATION

In order to preserve the energy of the gaussian window, the output current must be adjusted when the scale factor is varied. By comparing the ideal normalized gaussian window, in (2), and the relationship expressed by (10), it is clear that the current source I_G must be proportional to the term $1/s^{1/2}$ ($= I/I_\sigma^{1/2}$). For this purpose, the square root circuit shown in Fig. 5 allows us to generate the normalized control current, leading to

$$I_G = \frac{\sqrt{I_1^3}}{\sqrt{I_\sigma}} \quad (11)$$

where I_1 is a DC current, and will be fixed for proper operation of the circuit.

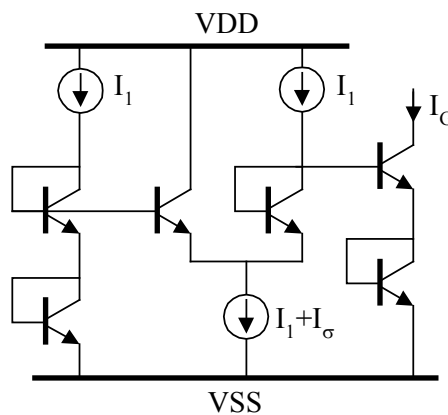


Figure 5. Circuit used to generate a current proportional to $I_\sigma^{-1/2}$

Replacing (11) in (10), the output current results in

$$i_{out} = \frac{\sqrt{I_1^3}}{\sqrt{I_\sigma}} e^{-\frac{4(i_x - i_\mu)^2}{I_\sigma^2}} \quad (12)$$

Note in this expression that i_{out} satisfies all the windowed function conditions in (2). In (12), the current source I_σ controls the scale parameter and the peak gain of the energy normalization scheme of the mother wavelet. The translation is adjusted by the current source i_μ . The complete circuit implementation is depicted in Fig. 6.

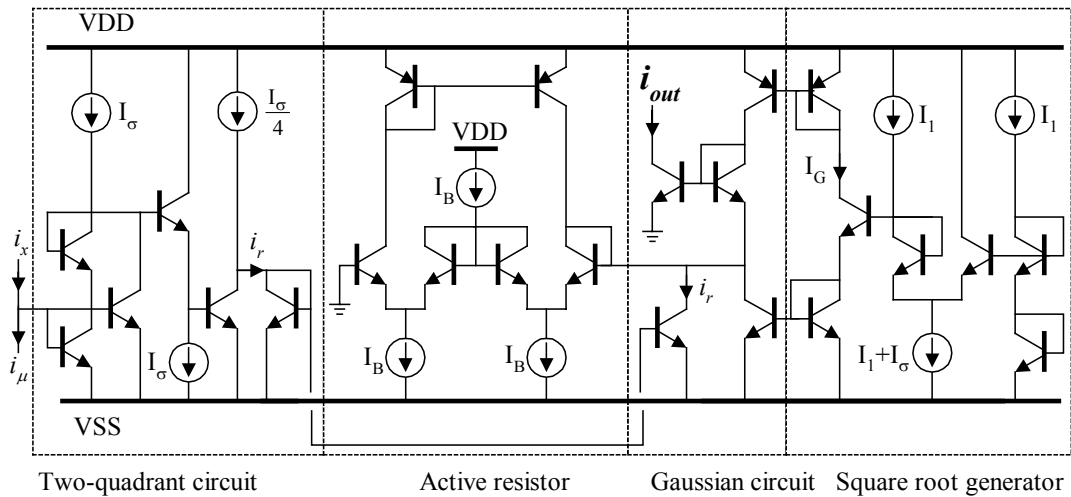


Figure 6. Normalized windowed gaussian function implementation for Morlet wavelets

In Fig. 7, the solid line corresponds to the Hspice simulated circuit's output current while the dashed line corresponds to the exact gaussian function given by eq. (12). The difference between these curves is less than 3%. Simulated results show that temperature variations in the range -50°C to +80°C produce output function deviations of less than ± 3%.

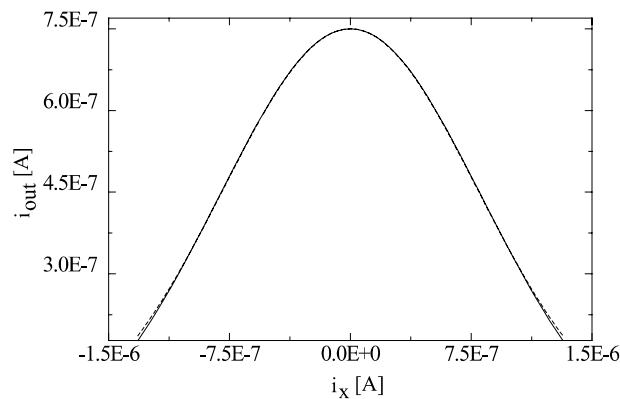


Figure 7. Output Current for both exact gaussian function (dashed line), and circuit (Hspice simulation)

For the Morlet wavelet implementation, (see equation 1) the sinusoidal input signal must be multiplied by the output of the normalized gaussian function circuit by a four-quadrant multiplier. The circuit shown in Fig. 8(a) realizes this function, which is an enhanced version of the circuit reported in [25].

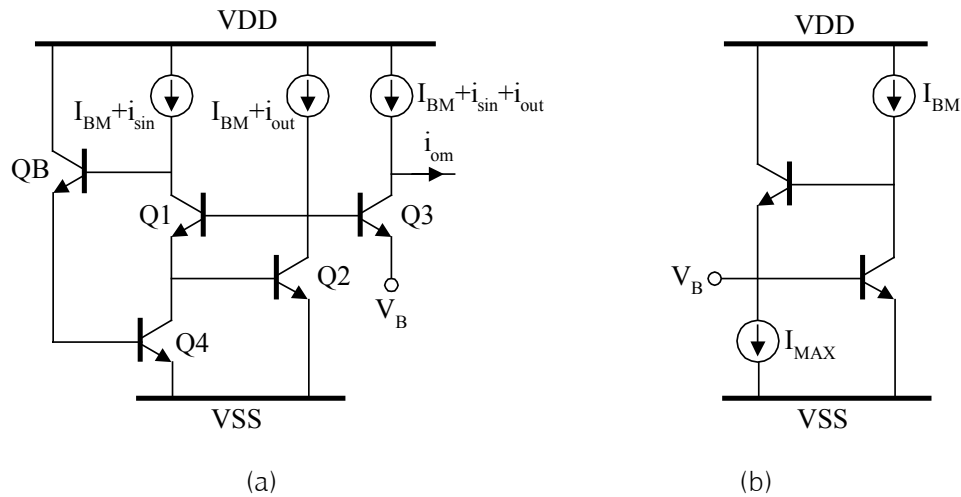


Figure 8. Four quadrant multiplier using common voltage V_B .
 a) Four quadrant multiplier. b) Basic voltage generator

The current source i_{sin} and i_{out} are the sinusoidal current source and the gaussian output current, respectively. Transistors Q1-Q4 carry out the multiplication. If $i_{sin}, i_{out} < I_{BM}$ and the β effects are neglected, the output current becomes

$$i_{om} = \frac{i_{sin} i_{out}}{I_{BM}} \quad (13)$$

The transistor QB is used to bias properly Q4. In order to minimize silicon area, the reference voltage V_B generated by the bias current I_{BM} can be shared in large systems. The basic principle for this voltage generator is depicted in Fig. 8b. For proper operation of the circuit, the current I_{MAX} must be large enough to carry multiple currents when several multiplier cells are connected to the common voltage V_B .

5. EXPERIMENTAL RESULTS

The architecture was implemented with discrete arrays of bipolar transistors ($\beta=100$). We show the experimental results obtained for the gaussian function circuit and the normalized gaussian window, respectively. Also, measurements for the imaginary component of the Morlet wavelet are presented. For these results, the supply voltages used were $\pm 1.5V$.

In order to show the versatility of the proposed Gaussian function generator, the I_G current generator circuit was disabled in the results presented in Figs. 9-11; these results correspond to the realization of equation (9). The bias conditions for the transistors were, $I_G=750$ nA, $I_B=500$ nA and $I_\sigma=2.5$ μ A.

The standard deviation/scale programmability by using current source I_σ is shown in Fig. 9; for these results I_σ was varied in the range 1.8 μ A-2.5 μ A. Note in this figure that neither the peak gain nor the symmetry of the gaussian function are affected. Measured results showing the peak gain programmability, by adjusting the current source I_σ , are depicted in Fig. 10. In these results, I_G was varied from 325-775 nA. Experimental results demonstrating the programmability of the mean value or the translation parameter by varying the current source i_μ are shown in Fig. 11.

For these results $i_{\mu}=0$ was used for the central curve, while $i_{\mu}=-1.4\mu\text{A}$ and $i_{\mu}=1.4\mu\text{A}$ were employed for the left and right-hand side plots, respectively.

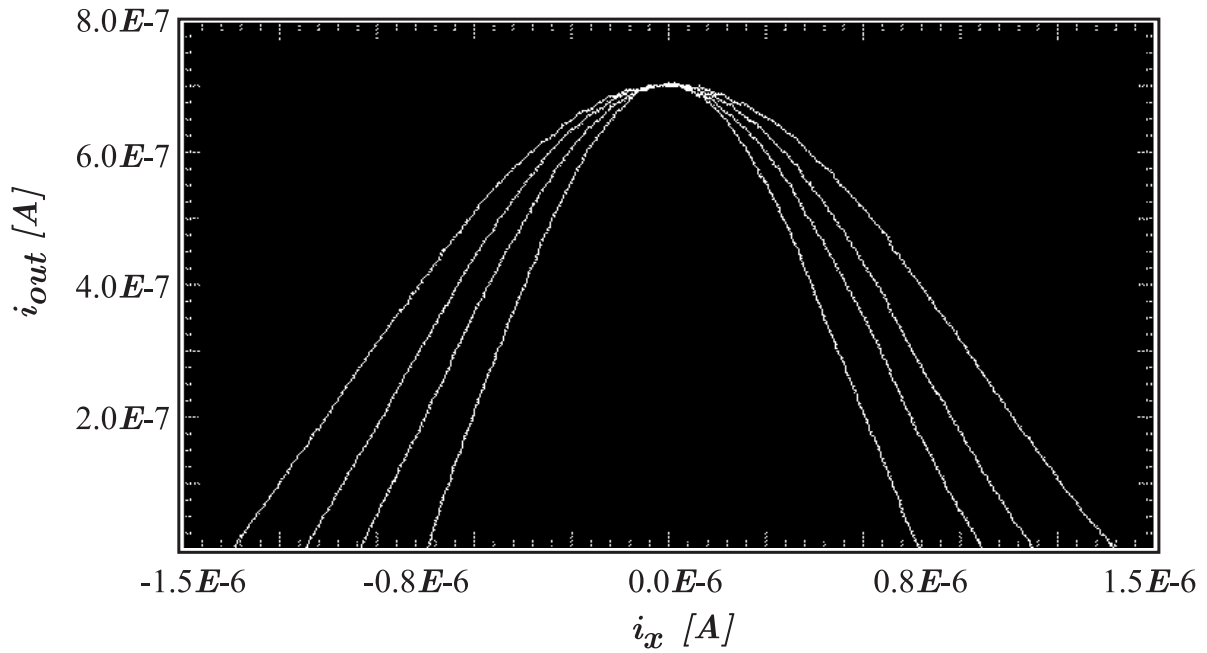


Figure 9. Standard deviation programmability for the gaussian function circuit: Experimental results

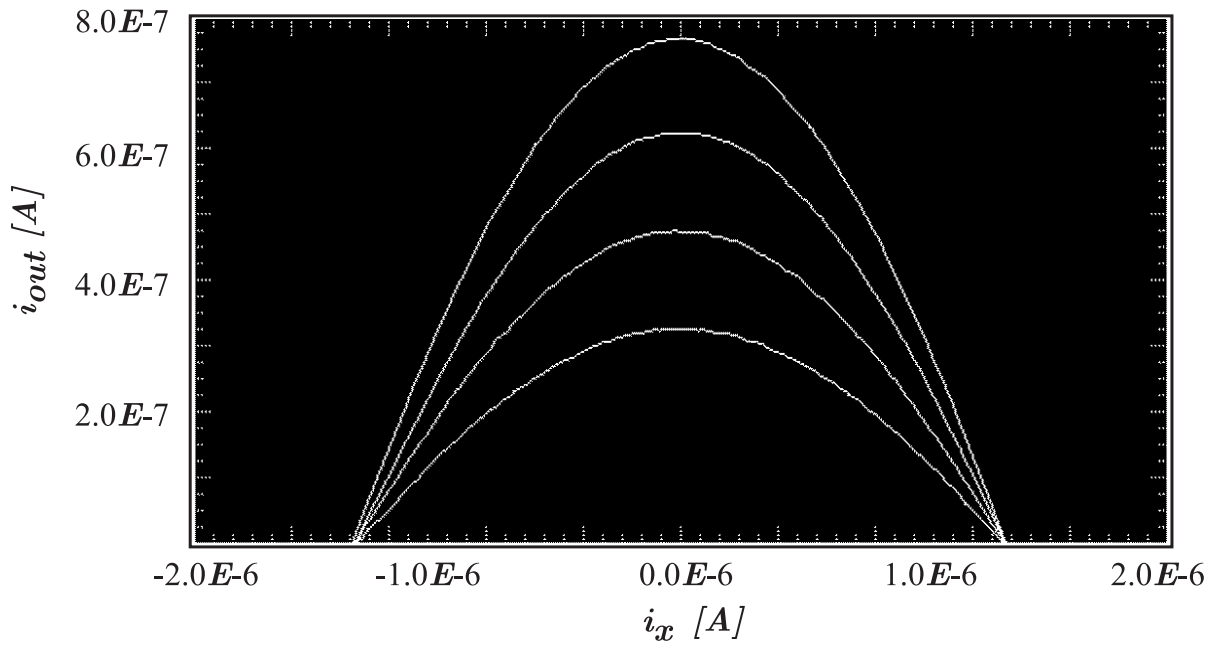


Figure 10. Experimental results showing the peak gain programmability of the proposed structure

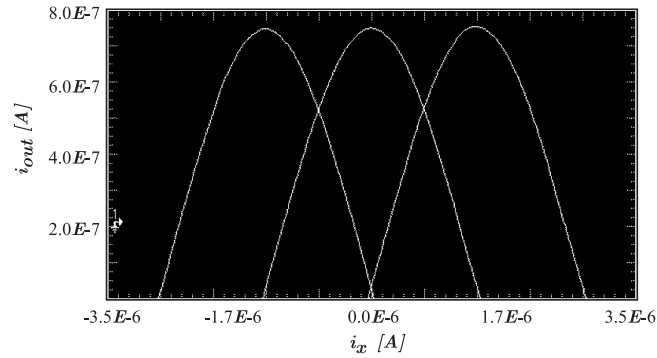


Figure 11. Experimental results: Programmability of the translation parameter

The results obtained for the Morlet wavelets are presented in Figs. 12-14. The results for the normalized windowed gaussian function with constant energy are sketched in Fig. 12. I_G was varied in the range $1.75\mu\text{A}$ to $6.72\mu\text{A}$; the effect of the energy normalization, I_G generator shown in Fig. 5, can be noted in these results. The bias conditions for these results were $I_I=1.9\mu\text{A}$, and i_μ was set to zero.

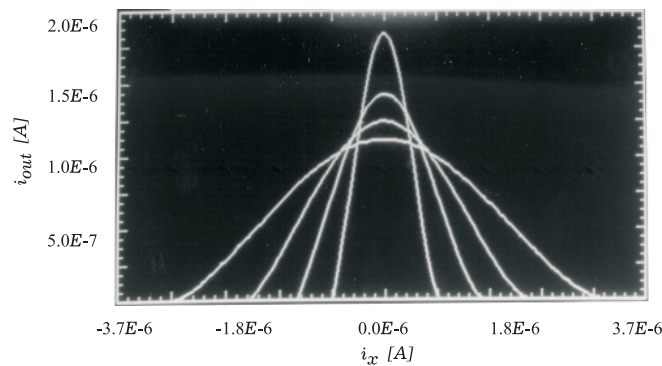


Figure 12. Experimental results: Output current for the gaussian function circuit including the energy normalization scheme

The imaginary component of the Morlet wavelet using the four-quadrant multiplier depicted in Fig. 8 is presented in Fig. 13. The time to current conversion was carried out using a 660Hz triangular input signal, and the frequency of the sinusoidal input was 5KHz.

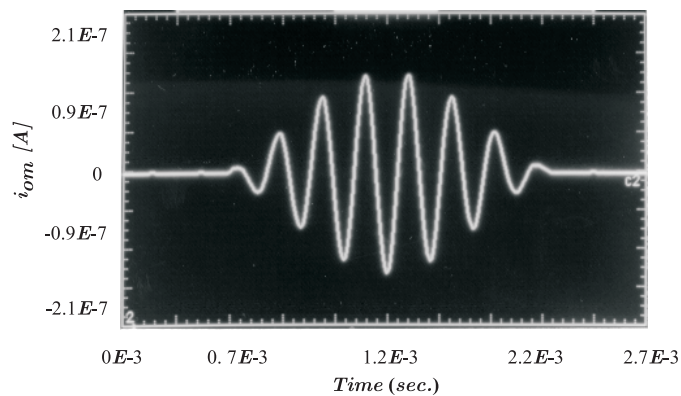


Figure 13. Experimental results: Imaginary component of the Morlet wavelet

The versatility of the proposed architecture is shown in Fig. 14; several imaginary components of the Morlet wavelet in the time domain are depicted. The design conditions and output current for these experimental results are summarized in Table I.

Table I. Experimental results for several imaginary components of the Morlet wavelet shown in Fig. 14

	f_{wavelet} (kHz)	I_{σ} (μA)	$f_{\text{sinusoidal}}$ (kHz)	i_{om} (nA _{pp})
Panel 1	1	2.1	7	500
Panel 2	0.66	3.4	5	300
Panel 3	0.49	5.0	3.3	240
Panel 4	0.33	7.1	2.3	200

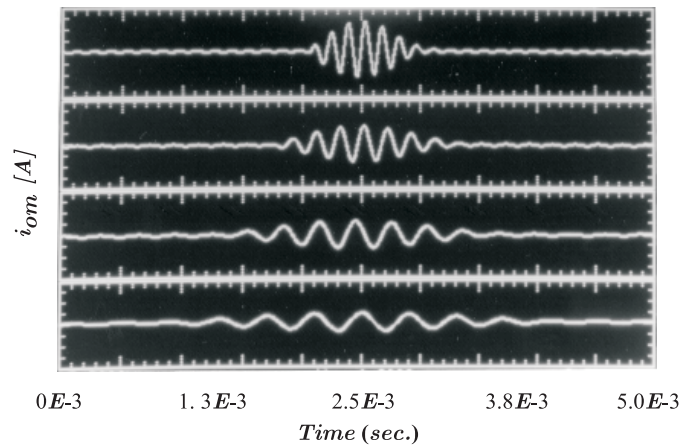


Figure 14. Experimental results: Several imaginary components of the Morlet wavelet. i_{om} is the output current

6. CONCLUSIONS

Circuits based on the translinear principle intended for the implementation of Morlet wavelets have been described. The main circuit parameters can be programmed independently by current sources. The proposed structure is precise, fully programmable, and relatively insensitive to both process parameters tolerances and temperature variations. Simulated results including temperature variations in the range of -50°C to 80°C have shown output function deviations of less than $\pm 3\%$. In addition, the proposed structure is compact, which makes it suitable for IC integration. Experimental breadboard results have demonstrated the feasibility of the proposed architecture. The building blocks can also be used for the implementation of many other non-linear functions.

7. REFERENCES

- [1] Sheng, Y. "Wavelet transform", in chapter 10 of A. D. Poularikas, eds., *The Transforms and Applications Handbook*, IEEE PRESS, 1996.
- [2] Daubechies, I. "The wavelet transform, time-frequency localization and signal analysis", *IEEE Transactions on Information Theory*, vol. 36, no. 5, pp. 961-1005, Sept. 1990.
- [3] Rioul O. and Vetterli M., "Wavelets and signal processing", *IEEE Signal Processing Magazine*, pp. 14-38, October 1991.
- [4] Unser M. and Aldroubi A., "A review of wavelets in biomedical applications", *Proceedings of the IEEE*, vol. 84, no. 4, pp. 626-638, April 1996.

- [5] Szu H. H., Hsu C. C., Thaker P. A. and Zaghloul M. E., "Image wavelet transforms implemented by discrete wavelet chips", *Optical Engineering*, vol. 33, no. 7, pp. 2310-2325, July 1994.
- [6] Lin J., Ki W. H., Edwards T. and Shamma S., "Analog VLSI implementations of auditory wavelet transforms using switched-capacitor circuits", *IEEE Transactions on Circuits and Systems I*, vol. 41, no. 9, pp. 572-583, Sept. 1994.
- [7] Vishwanath M., Owens R. M. and Irwin M. J., "VLSI architectures for the discrete wavelet transform", *IEEE Transactions on Circuits and Systems II*, vol. 42, no. 5, pp. 305-316, May 1995.
- [8] Vega-Pineda J., Cabrera S. D. and Chang Y. C., "VLSI implementation of a wavelet image compression technique using replicated coding/decoding cells", in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 1173-1176, 1995.
- [9] Schwarzenberg M., Traber M., Scholles M., Schuffny R., "A VLSI chip for wavelet image compression", in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 271-274, 1999.
- [10] Simon T. and Chandrakasan A. P., "An ultra low-power adaptive wavelet video encoder with integrated memory", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 572-582, April 2000.
- [11] Edwards R. T. and Cauwenberghs G., "A VLSI implementation of the continuous wavelet transform", in *Proc. IEEE International Symposium on Circuits and Systems*, 1996.
- [12] Moreira-Tamayo O. and Pineda de Gyvez J., "Analog computation of wavelet transform coefficients in real-time", *IEEE Transactions on Circuits and Systems I*, vol. 44, no. 1, pp. 67-70, Jan. 1997.
- [13] Justh E. W. and Kub F. J., "Analogue CMOS high-frequency continuous wavelet transform circuit", *Electron. Lett.*, vol. 35, no. 1, pp. 4-5, Jan. 1999.
- [14] Haykin S., "Neural networks (A comprehensive foundation)", IEEE Computer Society Press, 1994.
- [15] Christoyianni I., Dermatas E. and Kokkinakis G., "Fast detection of masses in computer-aided mammography", *IEEE Signal Processing Magazine*, vol. 17, no. 1, pp. 54-64, Jan. 2000.
- [16] Cauwenberghs G., Bayoumi M. and Sánchez-Sinencio E., Guest Editors, "Special issue: Learning on silicon", *Analog Integrated Circuits and Signal processing*, no. 2/3, vol. 18, Feb. 1999.
- [17] Card H. C., McNeill D. K. and Schneider C. R., "Analog VLSI circuits for competitive learning networks", *Analog Integrated Circuits and Signal processing*, no. 15, pp. 291-314, 1998.
- [18] Li M., McAllister H. G., Black N. D., and DePerez T. A., "Perceptual Time-Frequency Subtraction Algorithm for Noise Reduction in Hearing Aids", *IEEE Transactions on Biomedical Engineering*, vol. 48, no 7, pp. 979-988, Sept. 2001.
- [19] Angrisani L., Daponte P., and D'Apuzzo M., "Wavelet Network-Based Detection and Classification of Transients", *IEEE Transactions on Instrumentation and Measurement*, vol. 50, no 5, pp. 1425-1435, October 2001.
- [20] Churcher S., Murray A. F. and Reekie H. M., "Programmable analogue VLSI for radial basis function networks", *Electron. Lett.*, vol. 29, pp. 1603-1604, Sept. 1993.
- [21] Choi J., Sheu B. J., Chang J. C. F., "A gaussian synapse circuit for analog VLSI neural networks", in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 483-486, London, 1994.
- [22] Marshall G. and Collins S., "An analogue radial basis function circuit incorporating floating-gate devices", *Analog Integrated Circuits and Signal processing*, no. 11, pp. 21-34, 1996.
- [23] Gilbert B., "Current-mode circuits from a translinear viewpoint: a tutorial", in chapter 2 of C. Toumazou, F. J. Lidgley and D. G. Haigh, eds., *Analogue IC Design: The Current-Mode Approach*, IEE Peter Peregrinus Ltd: London, 1990.
- [24] Gilbert B., "The multi-tanh principle: a tutorial overview", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 2-17, Jan. 1998.
- [25] Meléndez-Rodríguez M. and Silva-Martínez J., "Compact building blocks for artificial neural networks", *Electron. Lett.*, vol. 35, no. 1, pp. 56-57, Jan. 1999.

Authors Biography



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Dr. Silva-Martinez has served as IEEE CASS Vice President Region-9 (1997–1998), and as Associate Editor for IEEE Transactions on Circuits and Systems part-II from 1997-1998 and May 2002-December 2003. Since January 2004 is serving as Associate Editor of IEEE TCAS Part-I. He is currently a member of the Editorial Board of the Journal of Applied Research and Technology (JART). He was the main organizer of the 1998 and 1999 International IEEE-CAS Tour in region 9, and Chairman of the International Workshop on Mixed-Mode IC Design and Applications (1997-1999). Among other distinctions, He was a co-recipient of the 1990 European Solid-State Circuits Conference Best Paper Award.