

Unified Processing Structure for Communication and Navigation signals in modems for lightweight satellite stations

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ABSTRACT

The present article shows the design and test of a unified-processing device for detection and demodulation of narrow and broadband communication signals, as well as navigation signals from GLONASS and GPS systems. The specific processing for each type of signal is described within the general framework of the proposed device. Performance indicators, such as symbol error probability (SEP) and energy losses, were computed using simulations of the device and the corresponding results are presented for discussion.

Keywords: satellite communications, satellite navigation, architecture, integration.

RESUMEN

En este artículo se muestran los resultados concernientes al diseño de un dispositivo de procesamiento unificado que permite detectar y demodular tanto señales de comunicación de banda angosta y banda ancha, como señales de navegación de los sistemas GLONASS y GPS. Se esclarece la especificidad de procesamiento para cada tipo de señal enmarcado en la estructura general del dispositivo. Los valores de probabilidad de error de símbolo y las pérdidas energéticas del sistema, obtenidos en un simulador del dispositivo, son presentados.

1. Introduction

In order to meet the demands of the latest generation of portable satellite terminals, it is needed to design hybrid systems able to receive and process both communication and navigation signals [1, 2], allowing the creation of aggregated location and navigation services to be offered to network users [3,4].

On Very Small Aperture Terminal (VSAT) and Ultra Small Aperture Terminal (USAT) the problem of receiving and processing communication and navigation signals is addressed using different subsystems for each type of signal [5]. However, in the literature no mention was found of a system designed to receive and process several communication and navigation signals under a single-joint processing framework. Therefore, novel methods to perform such unified processing of communication and navigation signals need to be explored.

The main objective of this article is to present the design of a software-defined radio (SDR) device [6,7] capable of detecting and demodulating narrow band (NB) and broadband (CDMA) communication signals as well as civilian navigation signals from GLONASS and GPS systems under a unified processing framework.

The specifics of the device are determined by the parameters of the signals being processed (Table 1) and by functional requirements. For communication signals, the device must be designed to operate under low signal-to-noise (SNR) ratios and with potentially large frequency deviations. With respect to navigation signals (NS), it must be taken into account that the GPS system has multiple access interference (MAI) of about -21.6 dB, which is much larger than the GLONASS system where it does not exceed -48 dB [8]. As a result, for processing GLONASS signals only the

thermal noise at the receiver was considered, while for GPS signals it was considered that the corresponding value from Table 1 includes the MAI.

2. Description of the unified signal processing system

The block diagram of the unified processing device (UPD) designed to process satellite communication and navigation signals depends on the types of signals, reception conditions, and electronic technology chosen for fabrication.

The following tasks must be performed to receive NB satellite signals with a UPD [9]: carrier synchronization, clock synchronization, and coherent demodulation. The working conditions force to assume a large initial carrier frequency deviation, therefore the carrier synchronization process must be preceded by a search process in a range surrounding the nominal carrier frequency.

In addition to the previous tasks, the reception of broadband CDMA communication and navigation signals with a unified device need to obtain the signal delay required to synchronize the CDMA code sequence that will be multiplied by the reference sequence [9]. Once synchronization is achieved, a despreading operation is performed on the original signal yielding a narrow band signal that is processed using the same stages described in the preceding paragraph.

To determine the UPD block diagram, the analysis of several different digital receivers performed in [9] as well as general design principles for satellite communication and navigation receivers [8-11] and the authors previous experience designing such systems were taken into account. As a result, the general block diagram shown in Figure 1 was highest processing speeds are performed by the analog processing block (APB). Meanwhile, a field programmable gate array (FPGA) is used for the quadrature digital components conformation (QDCC) operation, which requires intermediate processing speeds. This preprocessing reduces the speed requirements for the synchronization and demodulation operations that follow, then enabling the use of a relatively slow digital signal

processor (DSP). The design of a downconverter was not considered in the present work.

During operation, first the radio signal from the antenna enters the converter, where it is amplified, filtered and frequency downconverted. The output of the downconverter is an intermediate frequency (IF) signal in the 2.0–4.0 MHz range. It is assumed that the converter includes a gain control block to prevent overload resulting from high interference.

The output signal from the converter enters the analog-to-digital conversion and quadrature components conformation (ADC-QCs) system. The ADC-QC has two main components: the APB and the QDCC blocks. In the APB, first the CDMA's PSP signal and the reference signal are multiplied together, and then noise elimination is performed using a highly selective band-pass filter (BPF). For the reception of the NB signals, the multiplication operation is skipped. The frequency response of the BPF is chosen based on the bandwidth of the signal, possible frequency shifts, and desired attenuation of noise, user and cochannel interference. The QDCC block, described in [12], creates a complex signal, converts it to baseband, and reduces the sampling frequency through a decimating operation and a low-pass filter. The frequency response of the entire conversion and filtering process that is conducted by the ADC-QC system was determined using a simulation model and is shown in Figure 2. As it can be seen, the distortion on the pass band for any given transmission rate does not exceed 2 dB. Likewise, the attenuation in the stop-band is always greater than 40 dB.

Finally, the baseband signal is processed by the DSP, which performs the required operations according to the current operating mode of the station. The functions to be carried out by the DSP include: detection of the NB signals (search and detection for the case of CDMA signals), and demodulation (DEM) of the binary symbols. Additionally, the DSP performs all of the needed radio software algorithms like phase lock loop (PLL), clock synchronization (CS), automatic gain control (AGC), and delay tracking (DT) of the CDMA sequences.

	COMMUNICATION		NAVIGATION	
	NB	CDMA	GPS	GLONASS
Transmission rates, bps	1200, 2400, 4800, 9600		50	50
CDMA bandwidth, MHz	N/A	2.5	1.023	0.511
Number of CDMA subscribers	N/A	50	N/A	N/A
Type of CDMA assembly codes	N/A	Gold	m Sequences	Gold
Minimum SNR (signal-to-noise ratio plus interferences) dB	1.5	1.5	18.3	18.3
Frequency deviation, KHz	± 4		± 5	
Dynamic Range, dB	20			

Table 1. Parameters of the signals processed by the unified device.

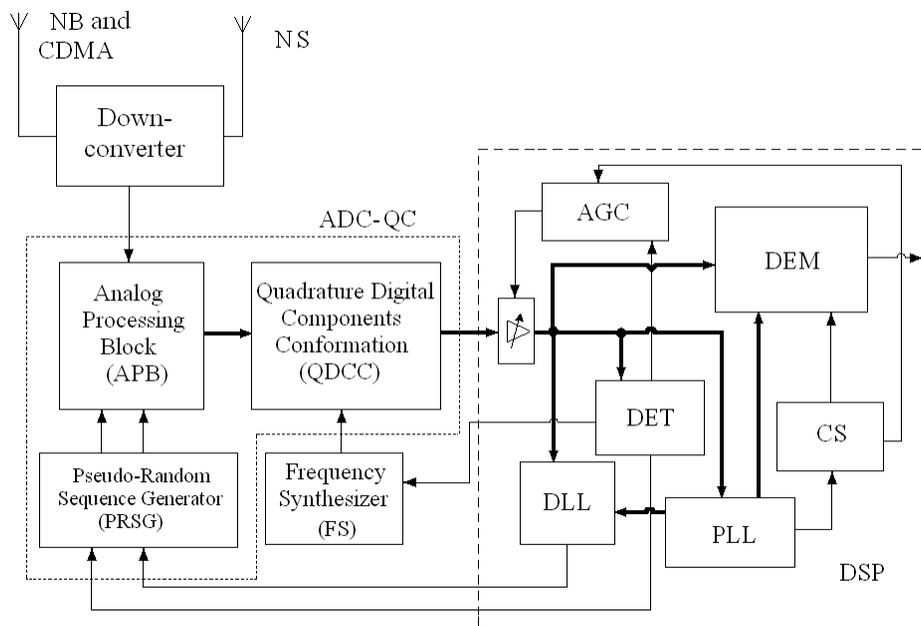


Figure 1. General block diagram of the unified signal processing device.

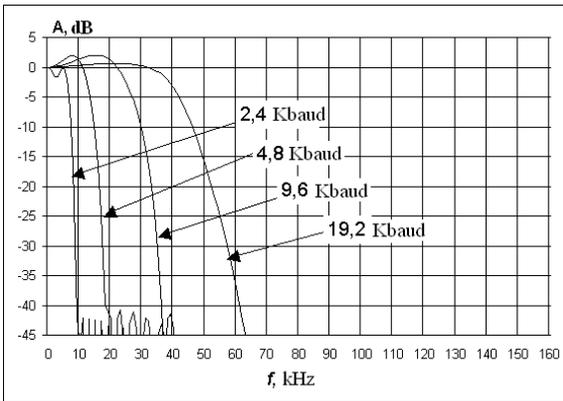


Figure 2. Total frequency response of the ADC-QC system.

3. Characteristics of the UPD during the reception of communication and Navigation signals

This section presents briefly the specifics of the processing for each type of communication and navigation signal, broad and narrow band, in the proposed structure. The processing of communication signals using BPSK modulation has been widely studied in the literature [13]. The block diagram of the unified structure for NB signals is shown in Figure 3. The output of the downconverter is fed to the APB where the only operation that is performed is the selective filtering by the BPF. The filter parameters were chosen based on the results from a simulation model of the filtering system, including the requirements mentioned in previous sections. Next, the filtered signal was transferred to the QDCC and then to the DSP.

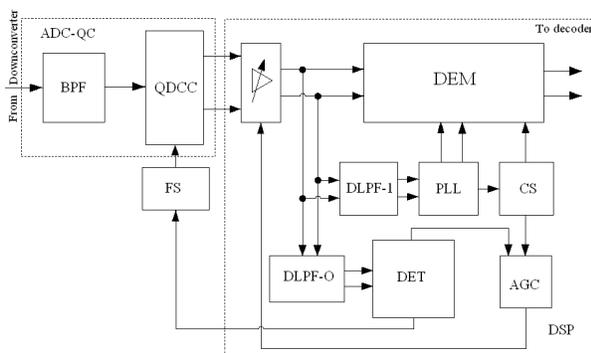


Figure 3. Narrow band signal processing in the UPD.

In the detector (DET), which has been extensively described in previous works [12, 14], the quadrature channels filtered by the DLPF-O are used to carry out signal detection. Also, any shift in the carrier frequency is estimated and used to fine-tune the frequency synthesizer (FS). The level of the received signal is also estimated at this stage and used to set an initial state for the AGC system. As a result, once signal detection is complete, the PLL and AGC blocks already have information to help them reduce their transient periods.

The PLL block, described in [15], begins to work after the signal is detected and its carrier frequency is estimated. The PLL decreases the error at the estimated carrier frequency to guarantee coherent signal detection. This error, as determined by the bandwidth of each channel of the Fourier processor, does not surpass 37.5 Hz at the maximum transmission rate. The DLPF-1 digital low-pass filter at the PLL input is matched to the BPSK signal and helps to decrease the variance of the noise.

The in-phase component of the PLL output is used in the clock synchronization system. Because a stable clock source is assumed in this type of system, it is possible to use simple synchronization schemes. For the UPD to function correctly, the system must guarantee the formation of a single time scale. In other words, the system must guarantee a single clock pulse sequence that corresponds to the real value of the received signal (NB, CDMA, and NS) for all transmission rates. Second, the system must keep the clock jitter within the norm, and, third, it must work correctly under low SNR conditions (1.5 dB). Such a system has been described in [16].

The quadrature components of the main channel at the output of the FIR filter in the QDCC are multiplied with the components of the PLL system. The in-phase component of the transformed signal enters an accumulator that is reset at the end of each bit time. This process marks the end of the demodulation algorithm. The instants of data sampling and accumulator resetting are determined by the control signals of the clock synchronization system.

The AGC block stabilizes the system, maintaining the quadrature components of the signal at a constant level within the different UPD channels. Next, Figure 4 illustrates the CDMA-BPSK signal treatment within the UPD. This block diagram has two channels with the same structure: a main channel and a complementary channel. During the search and detection stage of CDMA signals, the use of the second channel almost doubles the search speed [12]. During the demodulation stage, the complementary channel is part of the delay-locked loop (DLL) for delay tracking. The selection of a special channel, that is complementary to the primary channel, to measure the time delay is due to the processing algorithms that have been chosen for demodulation. In this particular case a CDMA sequence ($P(t)$) and its derivative ($P'(t)$) are needed as references [9]. These two sequences are formed in a single PRSG that uses the delay control signals as an input.

When processing CDMA signals the receiver must perform signal despreading. To this end, the signal at the last IF is multiplied in the APB by the CDMA sequence from the PRSG. During NB signal reception, the processing structure is maintained but the PRSG generates a constant level signal.

In the detection block, in addition to establishing the presence of signal and determining its frequency shift and signal level, the time difference (time delay) between the received CDMA sequence and its reference must be determined. In a similar manner to NB signals, the resulting estimated values for the aforementioned parameters are used to initialize the respective tracking and demodulation systems inside the UPD.

After signal detection, the CDMA sequence, $P(t)$, of the complementary channel is changed by its derivative $P'(t)$. After passing through the BPF and the QDCC, the quadrature components of this channel begin to participate in the formation algorithm to determine the delay in the DLL system. The final characteristics of the temporal delay discriminators are determined with the use of samples from the digital generator of the digital PLL system and of the quadrature components of the main channel signal.

The same system shown in Figure 4 is used for processing NS. In this case, the treatment of NS in the search and detection stage is different from that in the literature [8]. This different approach is used because an error has been guaranteed in the measurement of the Doppler shift frequency that does not surpass 10 Hz. This small amount of error allows the PLL system to lock and transition into tracking mode without an automatic frequency-locking loop (FLL) in the IF.

To unify processing algorithms, during NS reception it used the same operational mode than for CDMA communication signals at a rate of 2.4 Kbauds. Because the sampling frequency remains constant at 19.2 kHz, the number of samples per bit for this signal is 192. The same system that was used for the CDMA communication signals is used to demodulate NS signals; however, the structure of the code for the multiplication in the APB changes, depending on whether the APB receives a GPS or a GLONASS signal.

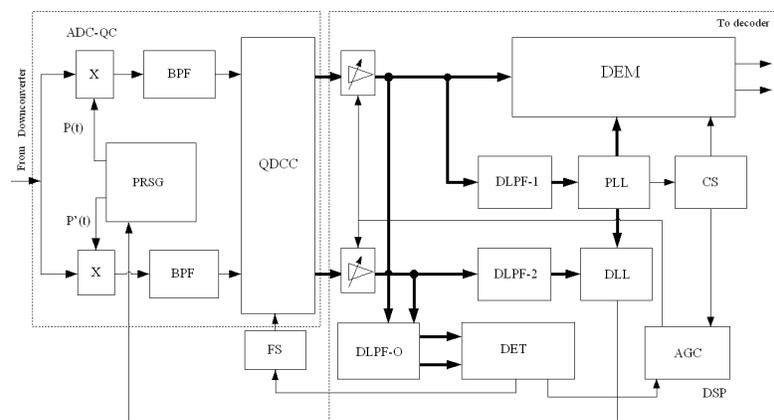


Figure 4. Broadband (CDMA and NS) signal processing in the UPD.

4. Results

To verify that the system functions properly, a simulation in Fortran was performed in which the UPD parameters were optimized for each operational mode. In addition, Monte Carlo experiments were designed to determine the energy loss (EL) curves for each of the signals that were used for testing. The EL was defined as the difference in dBs between the bit error rate (BERs) measured with the simulation model and the BERs computed theoretically [13]. The experiments were designed to prevent the error in BER estimation from surpassing 0.3%.

Figure 5 illustrates the results when the UPD receives NB signals at four different transmission rates. The results are shown for an ideal synchronization system (curve 1) and for actual synchronization system (curve 2), assuming only steady-state operation for the latter. For each experiment, 220,000 symbols were used. From Figure 5, it can be seen that for low values of E_b/N_0 , the EL does not surpass 0.55 dB. As the E_b/N_0 ratio increases, the EL decreases. It should be noticed that as the transmission rate increases, the synchronization system has less of an impact on the EL. Table 2 shows the results for BER and EL with $E_b/N_0 = 1.5$ dB. These results were determined using statistical experiments on the UPD simulator, with ideal (EI1 and EL1) and real (EI2 and EL2) synchronization systems. Note that during the comparison of these results, the ideal theoretical BER is 0.0427.

Tests with the simulator show then that the UPD can demodulate NB signals while guaranteeing an EL no greater than 0.82 dB with an $E_b/N_0 = 1.5$ dB for all transmission rates.

Figure 6 shows UPD performance during the reception of CDMA communication signals. These results were determined when the UPD input was under the influence of white noise and MAI by other users [13]. Figure 6 shows the EL of the system for each of the four transmission speeds used for the test. During the simulation, the PLL, DT, CS, and AGC systems were operating at steady-state.

From the figure it can be seen that as the E_b/N_0 ratio increases, the EL decreases. For the minimum value of E_b/N_0 , 1.5 dB, the EL reached its maximum, 0.93 dB for a transmission rate of $F_b = 2.4$ Kbauds. Using the system simulator, it was determined that the ELs introduced by the PLL, DT and SS blocks during the reception of the CDMA signals are approximately 0.4 dB for the minimum $E_b/N_0 = 1.5$ dB. EL due to the PLL, DT and SS also decrease as the transmission rate increase. For example, for $F_b = 19.2$ Kbauds, the EL is 0.2 dB.

In the present work, it was experimentally determined that it is not possible to model the effects of MAI as white noise while taking into account that all users have the same signal strength as the source.

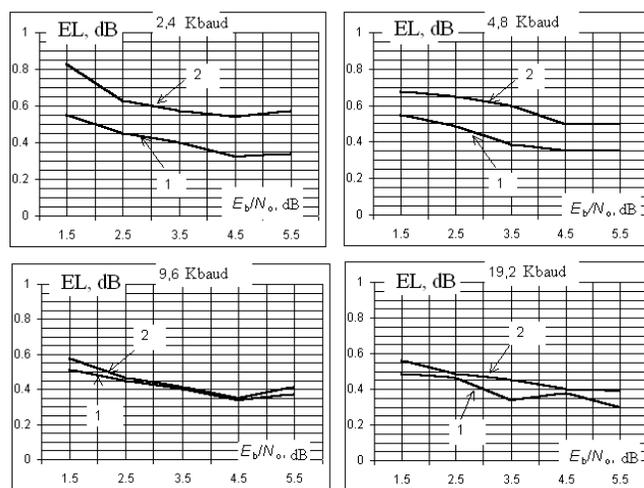


Figure 5. Energy losses (EL) for demodulation of NB signals as a function of the E_b/N_0 ratio, with 1) ideal and 2) real synchronization.

F_b , Kbaud	2,4	4,8	9,6	19,2
P_{e1}	0,0523	0,0523	0,0516	0,0512
EL1, dB	0,55	0,55	0,51	0,49
P_{e2}	0,0575	0,0547	0,0528	0,0525
EL2, dB	0,82	0,68	0,58	0,56

Table 2. BER and EL for NB demodulation with $E_b/N_0 = 1.5$ dB.

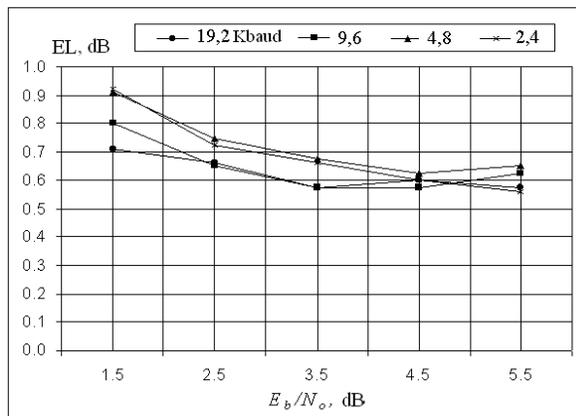


Figure 6. EL of the UPD during CDMA reception.

Table 3 shows the system's BER behavior when it is affected by internal noise and MAI. The test was performed using a transmission rate of 19.2 Kbaud and 46,200 symbols. Table 3 shows the values of the P_{enx} BER for cases in which the receiver input was jointly affected by channel noise and MAI. These values were obtained using a Monte Carlo-type experiment on the simulation model for two values of E_b/N_0 ratio (1.5 dB and 4.5 dB). For comparison, the E_1 BER with no MAI is also shown. Similar to the previous experiment, it was assumed that all of the users have the same signal strength as the source signal. Comparing the P_{enx} and E_1 probabilities, we observed that increasing the number of interfering users, n_{int} , causes the BER of the system to decrease. This effect is likely caused by partial self-compensation in the processing channel.

Finally, we determined how the system demodulates navigation signals. Using the system simulator, the BER was calculated for the NS

reception of GLONASS and GPS systems. During the experiment, it was assumed that there was no delay in the input signal and that the frequency of the signal was constant. The SNRs were established according to the characteristics of the terminals that were mentioned at the beginning of the article. A total of 100,000 symbols were used for this experiment. No errors were recorded for the two navigation systems. A simulation with greater number of symbols was not performed, as needed for high SNR values, because of computing limitations when running the Monte Carlo simulations on a personal computer.

E_b/N_0 , dB	P_{e1} , ($n_{int} = 0$)	n_{int}	P_{enx}
1,5	$5,53 \cdot 10^{-2}$	20	$5,13 \cdot 10^{-2}$
		30	$4,78 \cdot 10^{-2}$
		40	$4,40 \cdot 10^{-2}$
4,5	$1,28 \cdot 10^{-2}$	20	$1,10 \cdot 10^{-2}$
		30	$6,43 \cdot 10^{-3}$
		40	$4,33 \cdot 10^{-3}$

Table 3. P_{enx} BER when the receiver input contains the joint action of channel noise and MAI.

5. Conclusions

The present work proposed a unified structure for lightweight satellite stations, capable of performing analog-digital processing of narrow and broad band communication signals as well as navigation signals from GLONASS and GPS systems. The proposed scheme allows successful processing of communication signals for low E_b/N_0 ratios, near 1.5 dB, with energy losses that do not surpass 1 dB. These losses were found to decrease as the SNR increased.

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