

A Low-Complexity current-mode WTA circuit based on CMOS Quasi-FG Inverters

Circuito WTA en Modo de Corriente y Baja Complejidad, Basado en Inversores Quasi-FG en CMOS

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Abstract. In this paper, a low-complexity current-mode Winner-Take-All circuit (WTA) of $O(n)$ complexity with logical outputs is presented. The proposed approach employs a Quasi-FG Inverter as the key element for current integration and the computing of the winning cell. The design was implemented in a double-poly, three metal layers, 0.5 μ m CMOS technology. The circuit exhibits a good accuracy-speed tradeoff when compared to other reported WTA architectures.

Keywords. Winner-take-all, neural networks, analog circuits.

Resumen. En este artículo, se presenta un circuito "ganador toma todo" (WTA) de baja complejidad en modo de corriente con salidas digitales. La propuesta se basa en el uso de un inversor que utiliza la técnica de Quasi-FG, el cual, realiza una integración de corriente y el cómputo de la celda ganadora. El diseño fue implementado usando una tecnología de doble polisilicio y tres capas de metal para interconexión en tecnología CMOS de 0.5 μ m. El circuito presenta buena precisión y velocidad en comparación con otras arquitecturas WTA existentes.

Palabras clave: Ganador toma todo, redes neuronales, circuitos analógicos.

1 Introduction

A WTA is a circuit capable of identifying the highest value from a set of multiple input signals. Those circuits play an important role in the development of complex neural networks, fuzzy controllers and nonlinear systems. The first MOS WTA circuit introduced by Lazzaro (Lazzaro *et al.*), is shown in Figure 1. This compact circuit with current-mode inputs has a common connection, V_c , among cells, which causes the inhibitory behavior of those. The principle of operation can be explained as follows: for two different current inputs $I1=Im+\Delta I$ and $I2=Im$; the excess of current in $I1$ causes a voltage increment of V_c in transistor $T2_1$; this voltage rises until $I1$ is totally sinked through $T1_1$. Since transistors share a common gate voltage, the new V_c voltage origins that $T1_2$ sinks ΔI more current than $I2$ does, and therefore V_{o2} experiments a gradual decrease towards 0V approximately. This computation eventually produces a winner cell with a voltage output, V_o , different from zero.

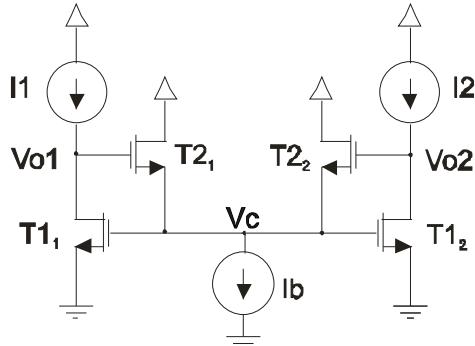


Fig. 1. Lazzaro's WTA with two cells

The main drawback of Lazzaro's approach lies on its low speed response. Many authors have proposed diverse improvements in order to obtain a higher processing rate; this is the case of (DeWeerth *et al.*), where a hysteresis loop is added and (Liu S. *et al.*), a common-source configuration stage improves the overall performance of the cell. Other Rank-Order Filters use voltage-mode WTA circuits of $O(n^2)$ complexity (Cilingiroglu U. *et al.*). In those approaches switched capacitor techniques and positive feedback are employed bringing interesting results. Nevertheless, large area and high power consumption, which must be avoided when implementing WTAs.

A voltage mode WTA of $O(n)$ complexity was proposed by Yamashita. (Yamashita *et al.*), Fig. 2.

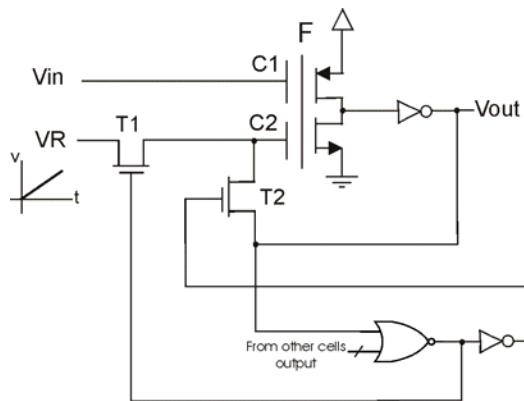


Fig. 2. Yamashita's WTA cell

For this WTA the potential at the Floating Gate (FG) inverter, F , is given by $V_{FG} = (C_1 V_{in} + C_2 V_R) / C_T$, since $C_1 = C_2$ and $C_T \approx C_1 + C_2$, the V_{FG} potential can be reduced to $V_{FG} = (V_{in} + V_R) / 2$. The WTA cell requires

two input voltages, a voltage ramp V_R and the voltage input V_{in} . This circuit works as follows, in the beginning when $V_R = 0$, the V_{FG} potential is lower than the threshold voltage V_{th} of F , in this case, every cell output voltage V_{out} is zero and the output of the NOR gate is a logic "high". This condition leads to transistor $T1$ to a conducting state. When V_R starts to rise, the cell with the largest V_{in} will fulfill first the threshold voltage V_{th} at the floating gate bringing a V_{out} high. In this case, the NOR gate will be zero leading $T1$ to cutoff, which guarantees a single winner cell. Then, transistor $T2$ is turned on closing the positive feedback loop and in this way the "winner" cell is latched with a logic high at the output. However, for many applications it is desirable a WTA circuit with current mode inputs, since in this mode the different inputs can be easily manipulated using Kirchoff Current Law before the WTA. A typical example is a Hamming Network which it is easier to be implemented in this mode (Li *et al.*). An important drawback of Yamashita's WTA is the external voltage ramp requirement for proper operation, which inevitably leads to a more complex circuitry. Furthermore, it has been demonstrated recently that real "floating" structures present trapped charge, which inevitably lead to an offset voltage at the FG with a given scattering among structures, unless an UV erasing technique is employed (Molinar-Solis *et al.*). In this sense, the Quasi-FG structures present less scattering and do not need extra erasing steps.

In the present work, authors introduce a current-mode WTA cell based on a similar principle, in this proposed approach, the input of the WTA cell is a sampled current I_{in} and each WTA cell generates a voltage ramp by means of a coupling capacitance connected to a Quasi-FG inverter and this condition will produce an eventually winning cell. The paper is organized as follows: the operation of the proposed WTA cell is described in section 2; PSpice simulations of a five cells array and their corresponding experimental results are presented in section 3 and 4, respectively; finally, the conclusions are established in section 5.

2 WTA Cell proposed

The key element of the WTA cell is the Quasi-FG Inverter F , Figure 3. The transistor $M1$ acts as a switch and combined with a Nand gate $N1$ is the inhibition part of the circuit. By means of the

potential V_{pre} through diode $D1$ the initial condition on the floating gate, $V_{FG}(0)$, is established. This diode $D1$ is implemented with a P^+ diffusion and an N-well.

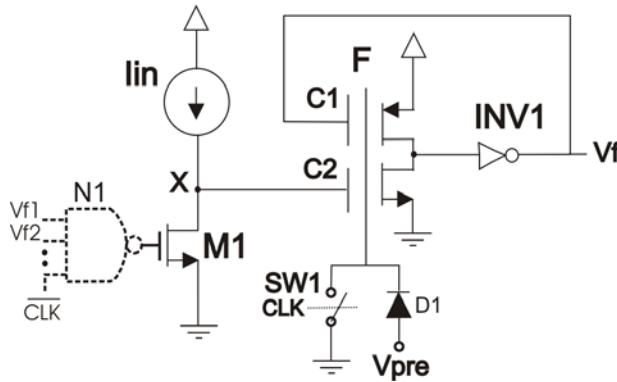


Fig. 3. The proposed WTA cell.

The FG potential, V_{FG} , for the capacitive inputs C_1 and C_2 , is given by:

$$V_{FG} = V_{FG}(0) + \frac{V_x \cdot C_2 + V_f \cdot C_1}{C_T} \quad (1)$$

Where V_x is the potential at node X ; C_1 and C_2 exhibit a value of 0.3pF for this particular case and C_T is the total FG capacitance including parasitics. The value of C_1 and C_2 is related with the parasitic capacitance calculation of the NMOS and PMOS transistors, commonly, $C_1 + C_2 \approx 0.9C_T$ must be fulfilled in order to neglect the parasitic capacitance contribution in (1).

The cell works in the following manner: a *clock* signal sets the initial condition, when it is “high”, $M1$ is on through the Nand gate $N1$ and eventually sinks the input current, Iin , Figure 4. $SW1$ is closed and the $V_{FG}(0)$ potential is fixed to GND. On the other hand, when the *clock* signal is ‘low’, $M1$ is off through $N1$ and the sampled current Iin begin its integration. At the same time, $SW1$ is opened fixing $V_{FG}(0)$ to a potential given by V_{pre} through $D1$. The total capacitance at node X neglecting parasitics is $C_x = C_2 || C_1 = 0.15\text{pF}$ and following the typical expression for a capacitor, the V_x at this node can

be calculated as $\int idt/C_x$. For the constant current Iin , $V_x(t)$ can be expressed as:

$$V_x(t) = \frac{Iin}{C_x}t \quad (2)$$

This denotes a ramp voltage whose slope is proportional to the magnitude of the sampled current. Using (2) in (1) the slope of V_{FG} will be given by:

$$\frac{dV_{FG}}{dt} = \frac{Iin}{C_1} \quad (3)$$

Thus, as the input current is integrated, the V_{FG} potential will increase until the inverter threshold voltage V_{th} is reached, when this happens Vf will be turned to a logic “high” and a positive feedback loop through C_1 will latch this logic value at Vf , even if V_x is lowered afterwards by $M1$.

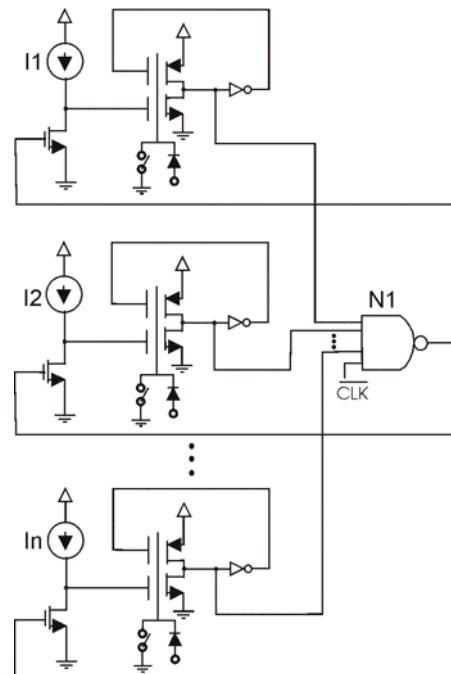


Fig. 4. A WTA with n inputs and the inhibition mechanism

When connecting an N -cells array, as illustrated in Figure 4, there will be a winning cell whose potential V_{FG} has locked its output with a “high” value. The rest of the cells remain inhibited and thus a single winner is attained. The inhibition mechanism is achieved through the use of the transistor $M1$ in the cell and the Nand gate $N1$. When a given cell has won, the output “low” from F activates the Nand gate, which, turns on the $M1$ transistor of every cell. This transistor act as a current sink for every constant input current I_{in2} , I_{in3} ,...etc. and in this way, the voltage V_x of these cells do not rise any longer and consequently the latched cell with the “high” output at V_f , will be the absolute winner.

It is important to address that V_{pre} must fulfill a value between $0 \leq V_{pre} < V_{th} + V_{drop}$, where $V_{drop} \approx 0.5V$ is a voltage drop present in $D1$ (Molinar-Solis *et al.*). This range for V_{pre} helps to preserve the V_{FG} initial condition bounded within $0 \leq V_{FG}(0) < V_{th}$. Ideally the maximum contribution of V_x to V_{FG} is $\frac{1}{2}V_{DD}$ and for this design, $V_{th} = 1.2V$, so, a $V_{FG}(0) > 0$ is necessary in order to V_{FG} be able to reach V_{th} ; in this case a $V_{pre} = 1V$ was considered. Also, $V_{FG}(0)$ must lie below V_{th} in order to guarantee that the output voltage, V_f , is initially at zero volts. Note that by switching $SW1$ to GND, the circuit breaks the positive feedback loop and reset the latches. The switch is implemented by means of an NMOS transistor.

The WTA response time is related to the input current magnitude, this is, the time it takes to V_{FG} to reach V_{th} from the initial condition $V_{FG}(0)$. According to (3), this is:

$$V_{th} - V_{FG}(0) = \frac{I_{in}}{C_1} (t_1 - t_0) \quad (4)$$

Where t_0 is the time when the integration is started, so if $t_0=0$, the response time is given by t_1 , this is:

$$t_1 = C_1 \frac{V_{th} - V_{FG}(0)}{I_{in}} = C_1 \frac{V_{dif}}{I_{in}} \quad (5)$$

With $V_{dif} = V_{th} - V_{FG}(0)$.

The WTA accuracy is related to the Quasi-FG inverter and Nand gate time response and when a given cell has won, the time associated to turn on

$M1$ is crucial. If another cell also reaches V_{th} before $M1$ is turned on, the WTA will latch more than one single winner. The time response of the Quasi-FG inverter and the Nand gate is around 3ns, so, a difference in time of ~8ns between de winning cell and the second closest cell must be fulfilled for proper operation.

This difference of 8ns has implications on the magnitude of the input currents, if i_1 is considered the magnitude of the input current of the winning cell, the second closest input current i_2 must hold:

$$i_2 \leq \frac{1}{\frac{1}{i_1} + \frac{8ns}{C_1 V_{dif}}} \quad (6)$$

From equation (5) and (6) can be noticed that the WTA accuracy and speed are inversely proportional.

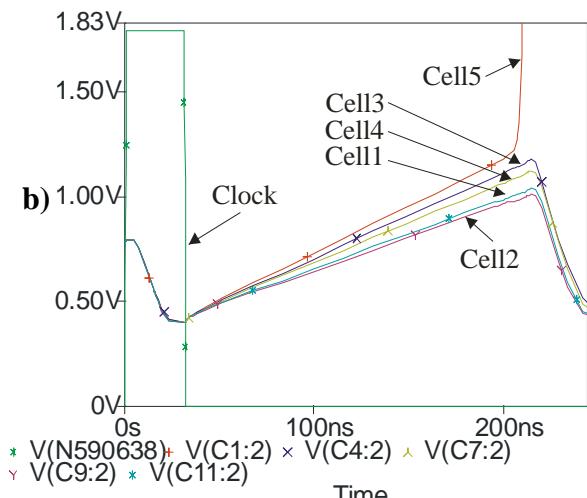
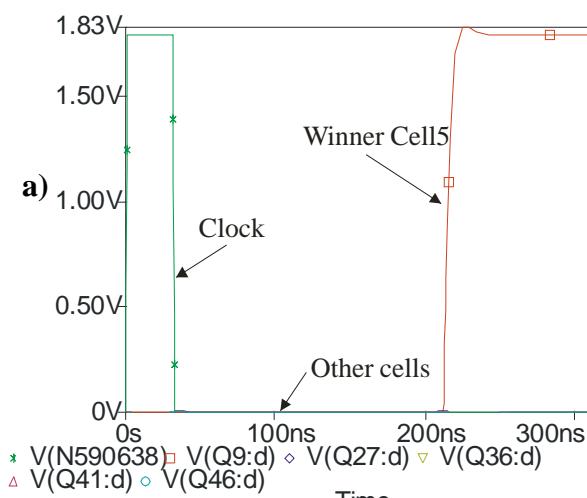
3 WTA simulations on PSpice

Simulations with PSpice were realized using $0.5\mu m$ technology parameters from MOSIS AMI foundry. A biasing voltage of 1.8V was employed. Different time domain simulations were performed. Here, a case with the following input currents values: cell1=1.05 μA , cell2=1 μA , cell3=1.32 μA , cell4=1.2 μA and cell5=1.45 μA , is presented. The different simulated cell outputs are presented in Figure 5a). All the V_{FG} potentials are plotted such that the different slopes can be distinguished, Figure 5b), the transistors aspect ratio is presented in Table 1.

According to the results obtained in simulation, an accuracy of 50nA, and a time response nearly to 183ns, with a power consumption of 3.2 μW per cell are achieved. Note that in our proposal, the voltage ramp at V_x is function of the input current and the C_1 capacitance, so the input current ranges for the circuit are limited by these two factors. The time response is also bounded by the input current, for small values, a larger time is necessary to overpass the threshold voltage V_{th} of the Quasi-FG inverter.

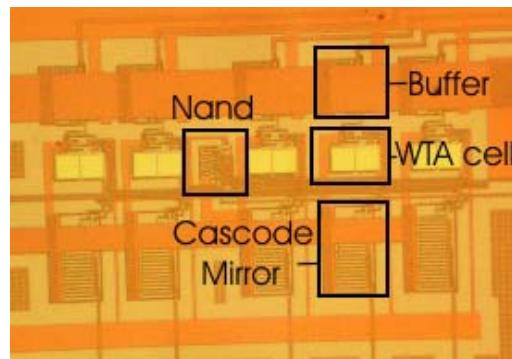
Tabla 1. Transistor sizes for a WTA cell

WTA cell	Transistor	Aspect Ratio
<i>F</i>	PMOS	3 μ m/1.5 μ m
	NMOS	1.5 μ m/1.5 μ m
<i>INV1</i>	PMOS	6 μ m/1.5 μ m
	NMOS	6 μ m/1.5 μ m
<i>M1</i>	NMOS	2.1 μ m/1.5 μ m
<i>SW1</i>	NMOS	1.5 μ m/1.5 μ m

**Fig. 5.** Time domain simulations of a five cells array using PSpice, a) The logic cell outputs, b) The V_{FG} slopes

4 Experimental Results

A prototype chip was fabricated on AMI 0.5 μ m through MOSIS, five cells were fabricated and tested. Figure 6. The input currents were introduced to each cell by using a cascode current mirror with aspect ratio 44:1, so, reducing the input current by the same factor. Thus, input currents can be easily handled outside the chip and introduced with an external current source.

**Fig. 6.** Microphotograph of the five WTA cells

In order to reduce the charge effects due to the oscilloscope probes and PCB parasitic capacitances, a digital output buffer was also included in the cell. This buffer consists of a chain of four inverters, where the first stage is aspect ratio is PMOS 3.6 μ m/0.6 μ m and the NMOS 1.5 μ m/0.6 μ m, each subsequent inverter has a larger channel width multiplied by a factor of three with respect the previous inverter. Exhaustive measurements were made; the WTA circuit presents a good performance. One of the measurements was considered with the same conditions as the simulation presented: $I_1=1.05\mu$ A, $I_2=1\mu$ A, $I_3=1.32\mu$ A, $I_4=1.2\mu$ A, $I_5=1.45\mu$ A. The circuit was tested as simulations with $V_{DD}=1.8V$ with a *Clock* signal of 1MHz. From all input currents, the winning cell should be the number five. The output response of cell5 measured with a digital oscilloscope is presented in Figure 7a).

The output response of cell1 after input I_5 , I_4 and I_3 are disabled, i.e. $I_5=I_4=I_3=0\mu$ A, is shown in Figure 7b). The cell1 brings correctly an output high, and cell2 is inhibited, afterwards I_1 is disabled also, and cell2 brings a logic high as the new winner, Figure 7c). The difference between cell1 and cell2 is as in simulations of about 50nA.

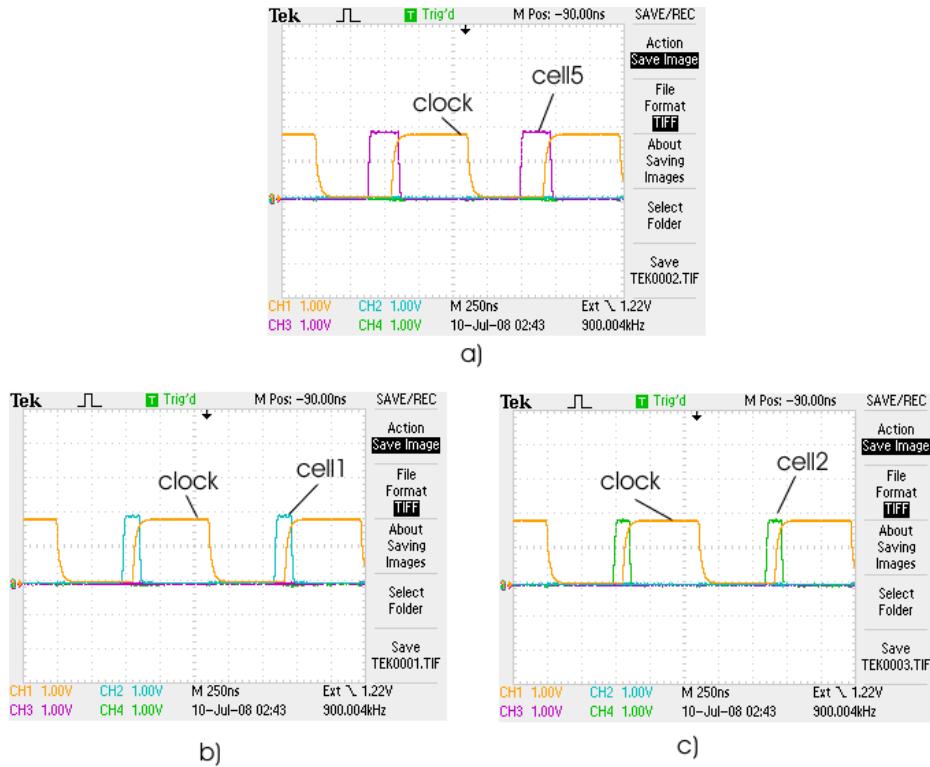


Fig. 7. Experimental results, a) Response of cell5, b) Response of cell1 with I5, I4 and I3 disabled, c) Response of cell2 after all other input currents are disabled

Comparisons among recent different current-mode WTAs previously reported are shown in Table 2. Of those, the structures of Fish and Chieng-Cheng exhibit a good accuracy and response time.

However, the proposed cell presents a good accuracy-speed trade-off and it is able to work in low-voltage applications.

Table 2. Other recent current mode wta with digital output

Circuit	(Massari et al.)	(Fish et al.)	(Chieng-Cheng et al.)	This work
Voltage Supply	3.3V	3.3V	3.3V	1.8V
Accuracy	200pA(sim.)	30nA(meas.)	20nA(sim.)	50nA(meas.)
Response Time	~2.5μs	8-32ns	-	~480ns
Power Consumption	16.5μW array	87.5μW per cell	-	3.2μW per cell
Technology	-	0.35μm	0.35μm	0.5μm

5 Conclusion

A novel current-mode WTA circuit for low-voltage applications has been introduced. Since the WTA core is a Quasi-FG CMOS push-pull inverter, the circuit is allowed to work with voltages near to the sum of the complementary threshold voltages $V_{TN} + V_{TP}$, in this case 1.8V.

The approach makes use of a small transistor count per cell and the experimental measurements show an accuracy of 50nA despite the slow response. This condition could be related to parasitic capacitances from the printed circuit board, since an important difference exists when is compared with the simulations. The obtained electrical features can be compared with other recent WTA circuits reported.

Acknowledgments

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